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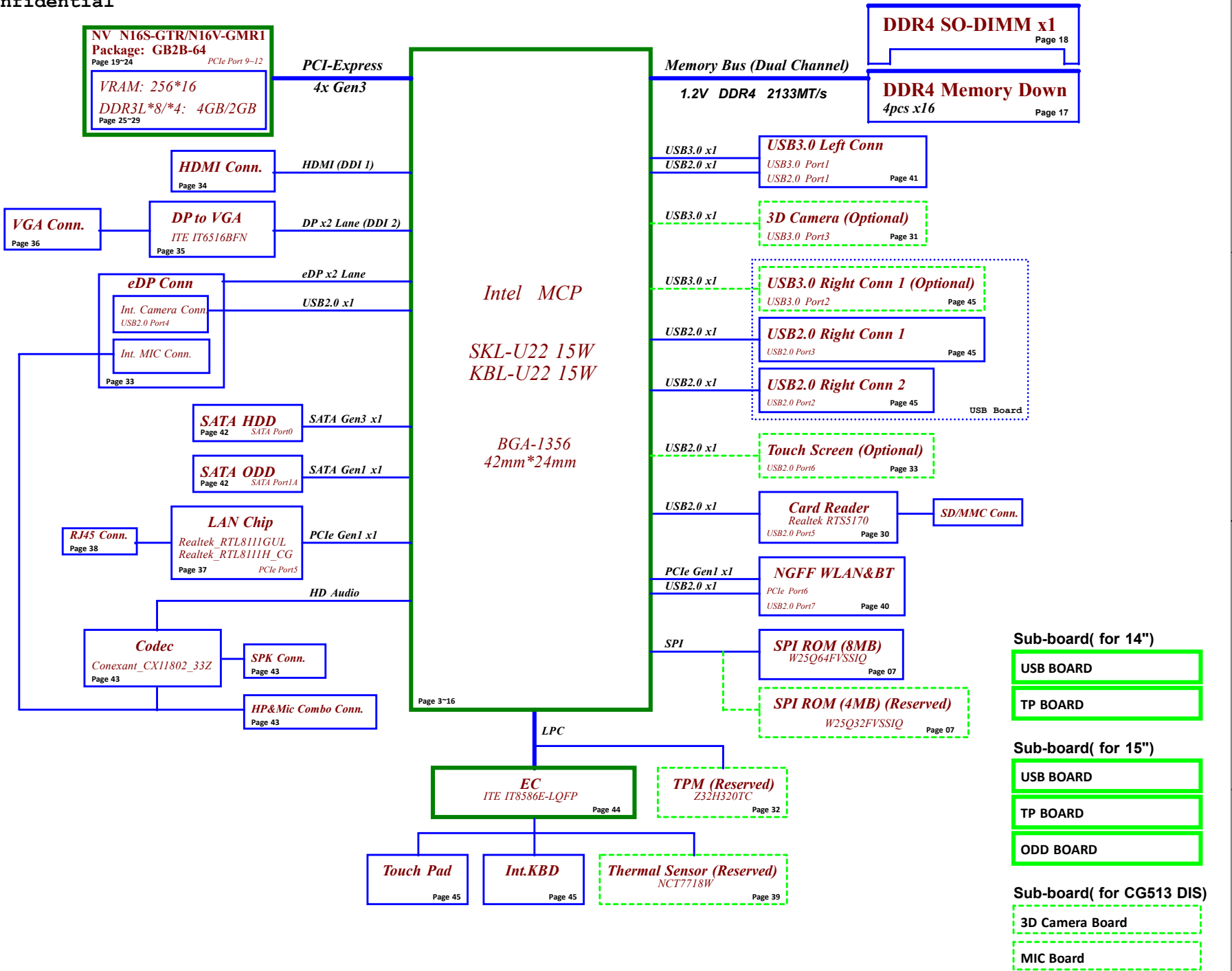
CG413/CG513 MB Schematics Document

Intel Skylake-U22/Kabylake-U22 with DDR4 + Nvidia N16S-GTR/N16V-GMR1 GPU

2016-06-12

REV:1.0

Security Classification	LC Future Center Secret Data			Title			
Issued Date	2015/08/20	Deciphered Date	2016/08/20	Cover Page			
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Voltage Rails (O --> Means ON , X --> Means OFF)

Power Plane / State	V20B+	+3VALW +5VALW +3VALW_PCH +1.8VALW +1.0VALW	+1.2V +2.5V_DDR +VCCST	+5VS +3VS +VCCIO +VCCSTG +VCCSA +VCC_GT +CPU_CORE +0.6VS
S0	O	O	O	O
S3	O	O	O	X
S3 Battery only	O	O	O	X
S5 S4 AC Only	O	O	X	X
S5 S4 Battery only	O	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X

SMBUS Control Table

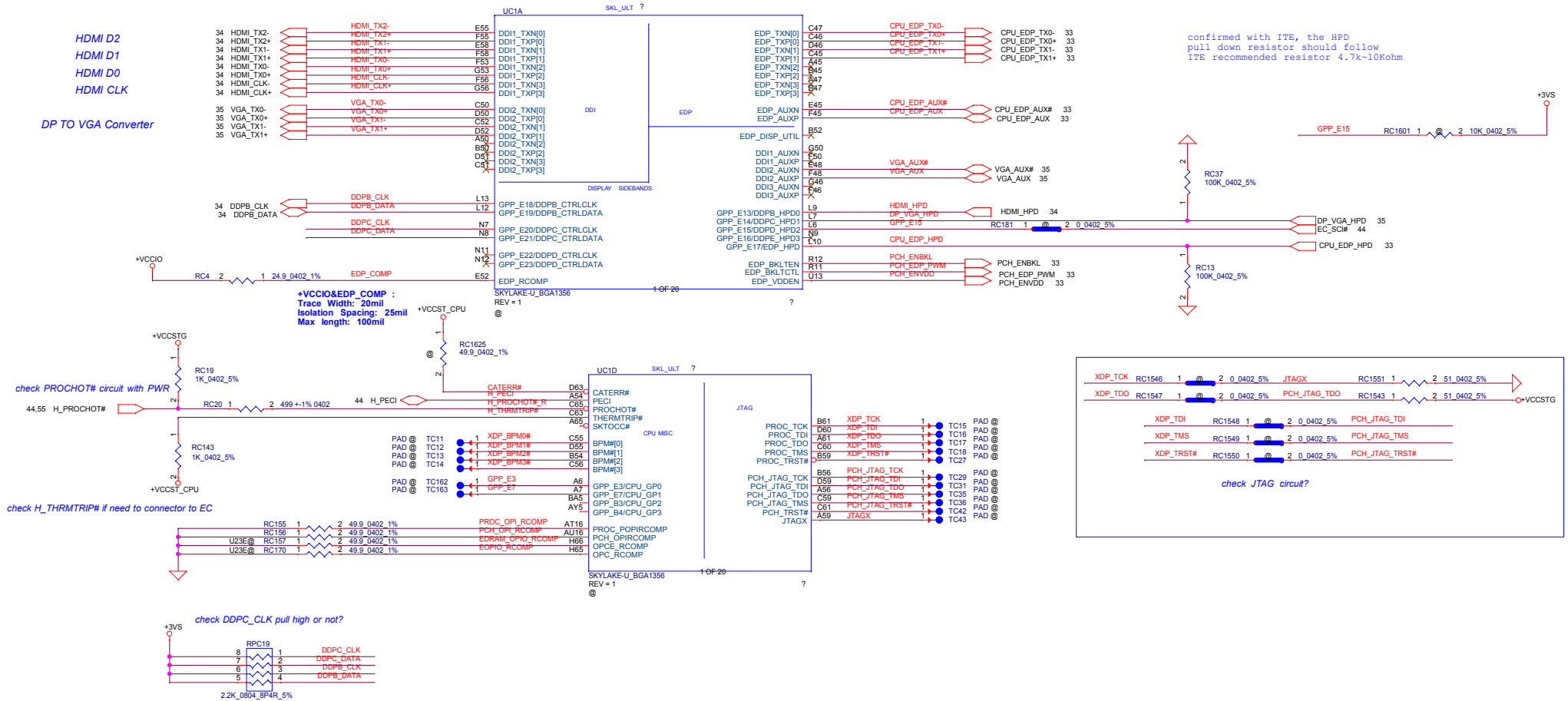
	SOURCE	BATT	Charger	DGPU	IT8586E	Memory Down	PCH	PMIC	SODIMM	Thermal Sensor	WLAN WiMAX
EC_SMB_CK1 EC_SMB_DA1	IT8586E +3VL_EC	V	V	X	V +3VL_EC	X	X	X	X	X	X
EC_SMB_CK2 EC_SMB_DA2	IT8586E +3VS	X	X	V +3VG_AON	V +3VS	X	V +3VALW_PCH	X	X	V	X
EC_SMB_CK3 EC_SMB_DA3	IT8586E +3VL_EC	X	X	X	V +3VL_EC	X	X	V	X	X	X
PCH_SMB_CLK PCH_SMB_DATA	PCH +3VALW_PCH	X	X	X	X	X	V +3VALW_PCH	X	V +3VS	X	V +3VS

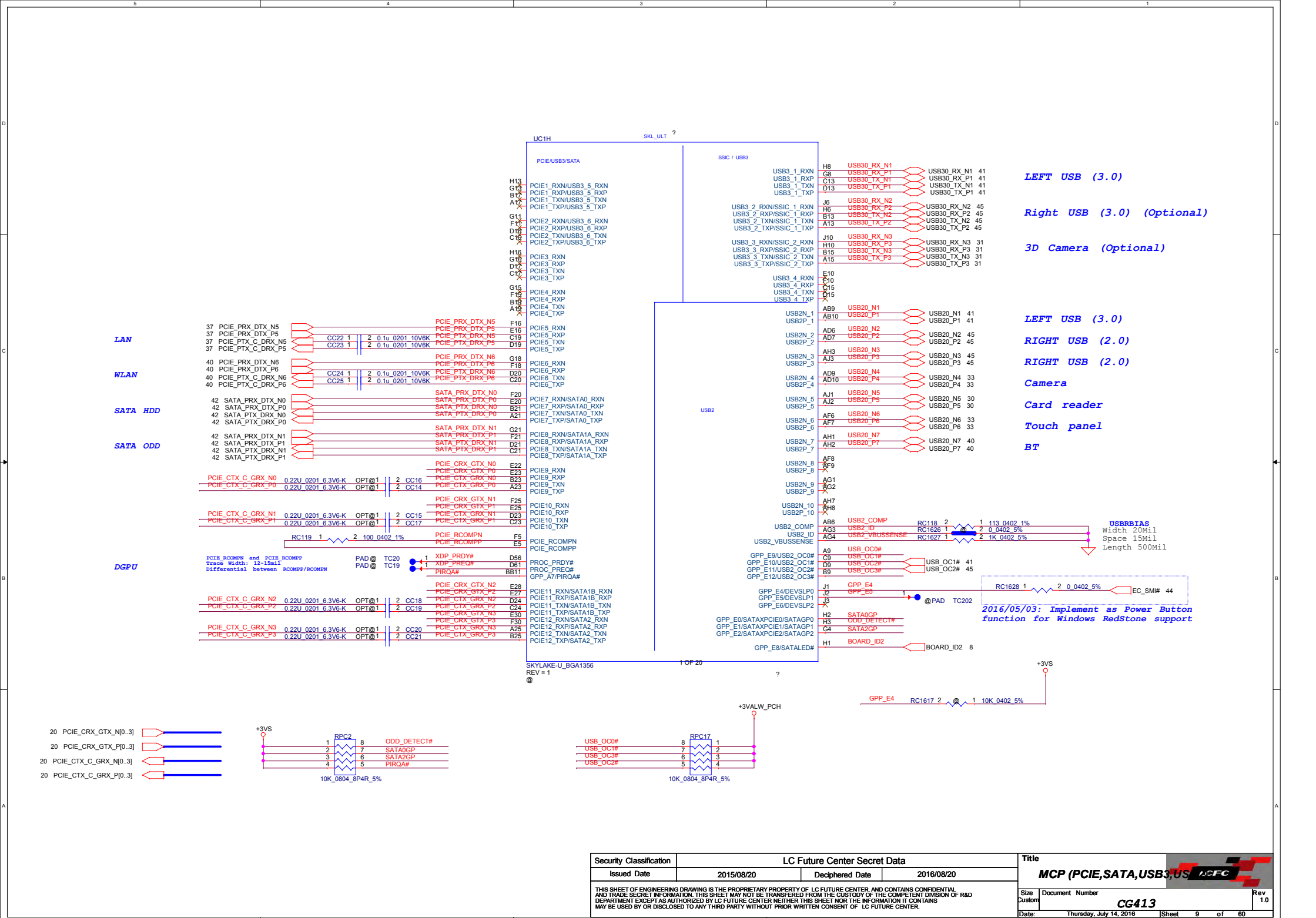
EC SMBus1 address EC SMBus2 address EC SMBus3 address PCH SM Bus address

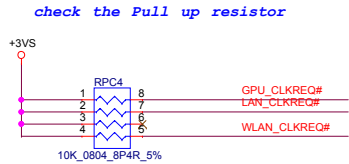
Device	Address	Device	Address	Device	Address	Device	Address
Smart Battery	need to update	Thermal Sensor(NCT7718W)	1001_100xb	DDR4 SODIMM	need to update	Wlan	Reserved
Charger	0001 0010 b	PCH	need to update				
		DGPU	need to update				

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

HSIO PORT	Function	BOM Structure	BTO Item
USB3.0	1 USB3.0 Conn Left	@	Not stuff
	2 USB3.0 Conn Right(optional)	14@	For 14" part
	3 3D Camera(optional)	15@	For 15" part
	4 NC	14or15@	For 14" or 15" part
	5 NC	14or17@	For 14" or 17" part
	6 NC		
USB2.0	1 USB3.0 Conn Left		
	2 USB2.0 Conn1 Right	Cannonlake@	For Cannonlake part
	3 USB2.0 Conn2 Right	CD@	For C cost down
	4 Camera	DUALMIC@	For Dual MIC part
	5 Cardreader	EMC@	For EMC part
	6 Touch Panel	EMC_15@	For EMC 15" part
	7 Bluetooth	EMC_NS@	For EMC nu-stuff part
	8 NC	EMC_PX@	For EMC PX part
	9 NC	EMC_PXNS@	For EMC PX nu-stuff part
	10 NC	ES@	For ES CPU
PCIE	1 NC	EXO@	For EXO GPU
	2 NC		
	3 NC	ME@	For ME part
	4 NC	NTS@	For nu-touch part
	5 LAN		
	6 WLAN		
	7 used as SATA		
	8 used as SATA		
SATA	9-12 x4 PCIE	PX@	For PX part
	0 HDD	RANKA@	For VRAM rank A part
	1A ODD	RANKB@	For VRAM rank B part
	1B used as PCIE	Realtek SD@	For Realtek SD part
	2 used as PCIE	SINGLEMIC@	For single MIC part
		SINGLERANK@	For single VRAN rank part
		DUALRANK@	For dual VRAN rank part
		TS@	For touch screen part
		TPM@	For TPM part
		UMA@	For UMA part



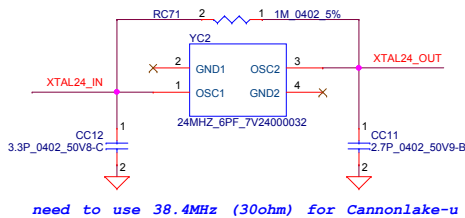
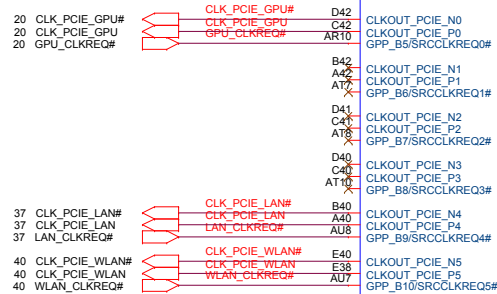




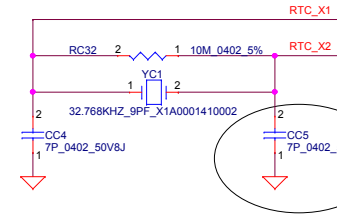
PCIE CLK0 DGPU

PCIE CLK4 LAN

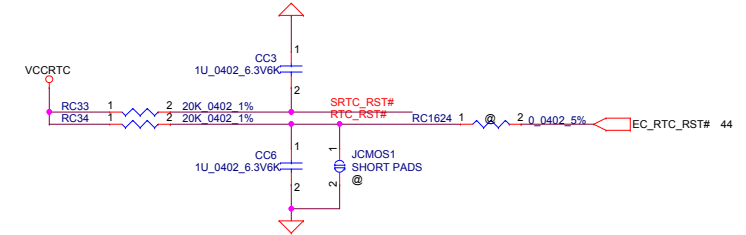
PCIE CLK5 WLAN

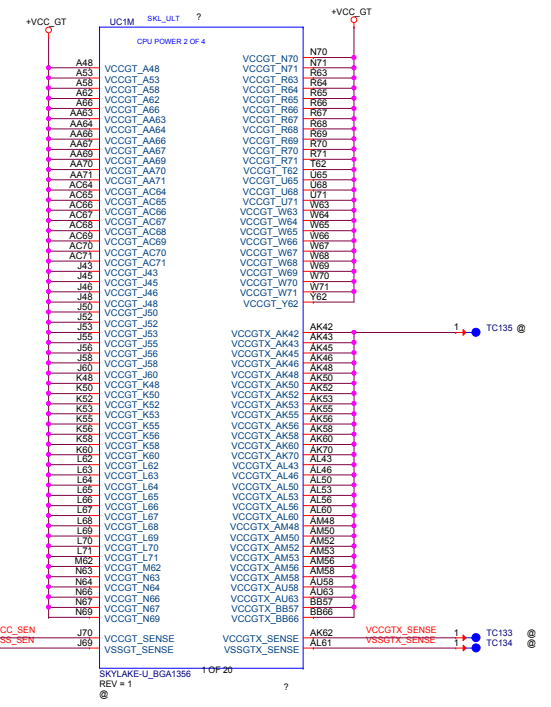
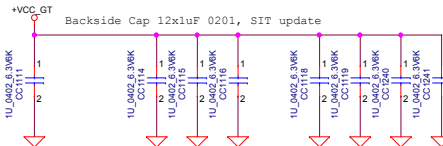
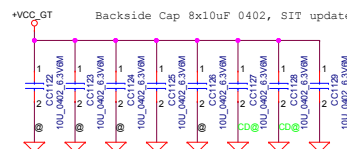
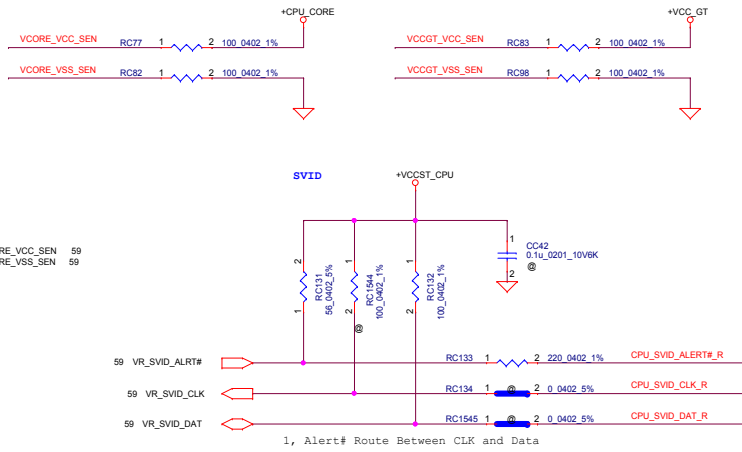
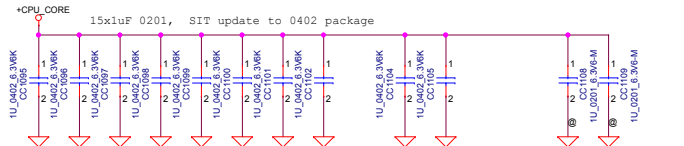
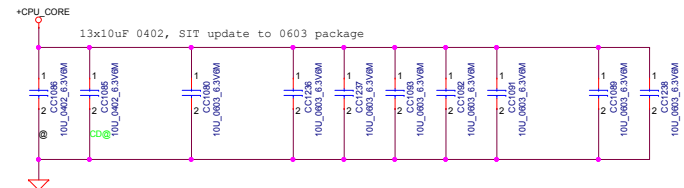
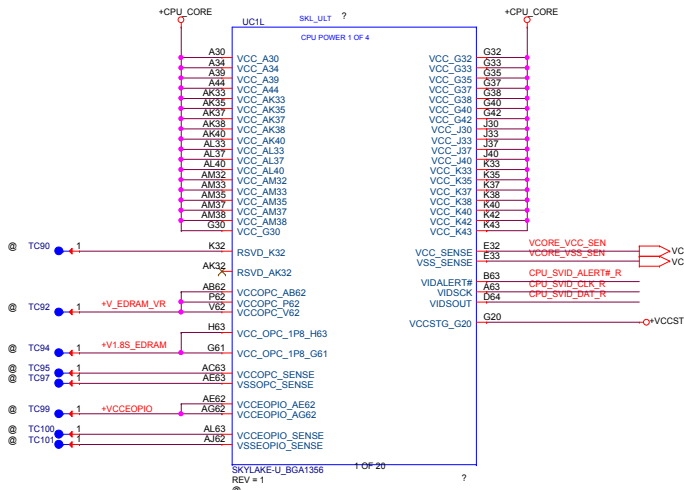


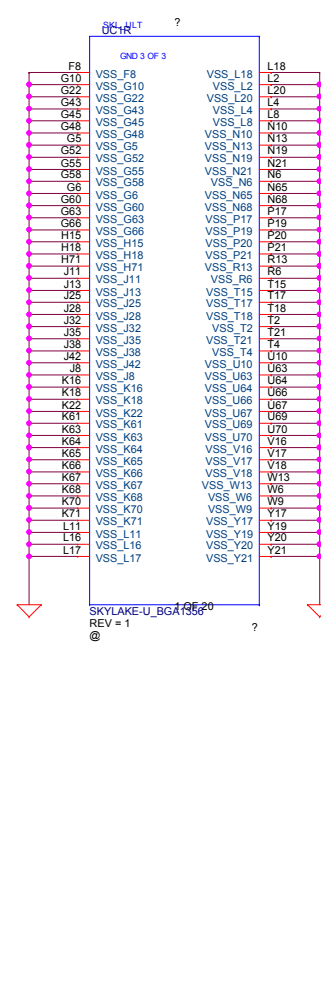
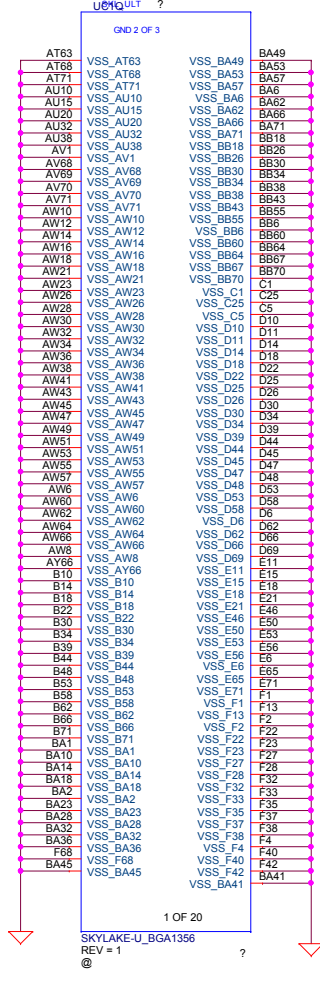
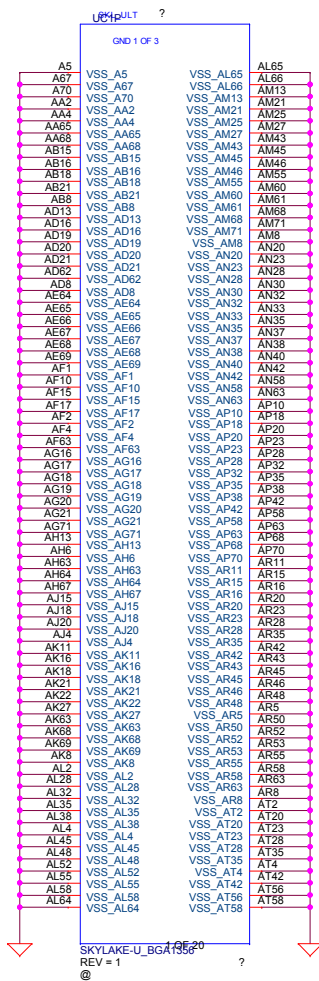
need to use 38.4MHz (30ohm) for Cannonlake-u



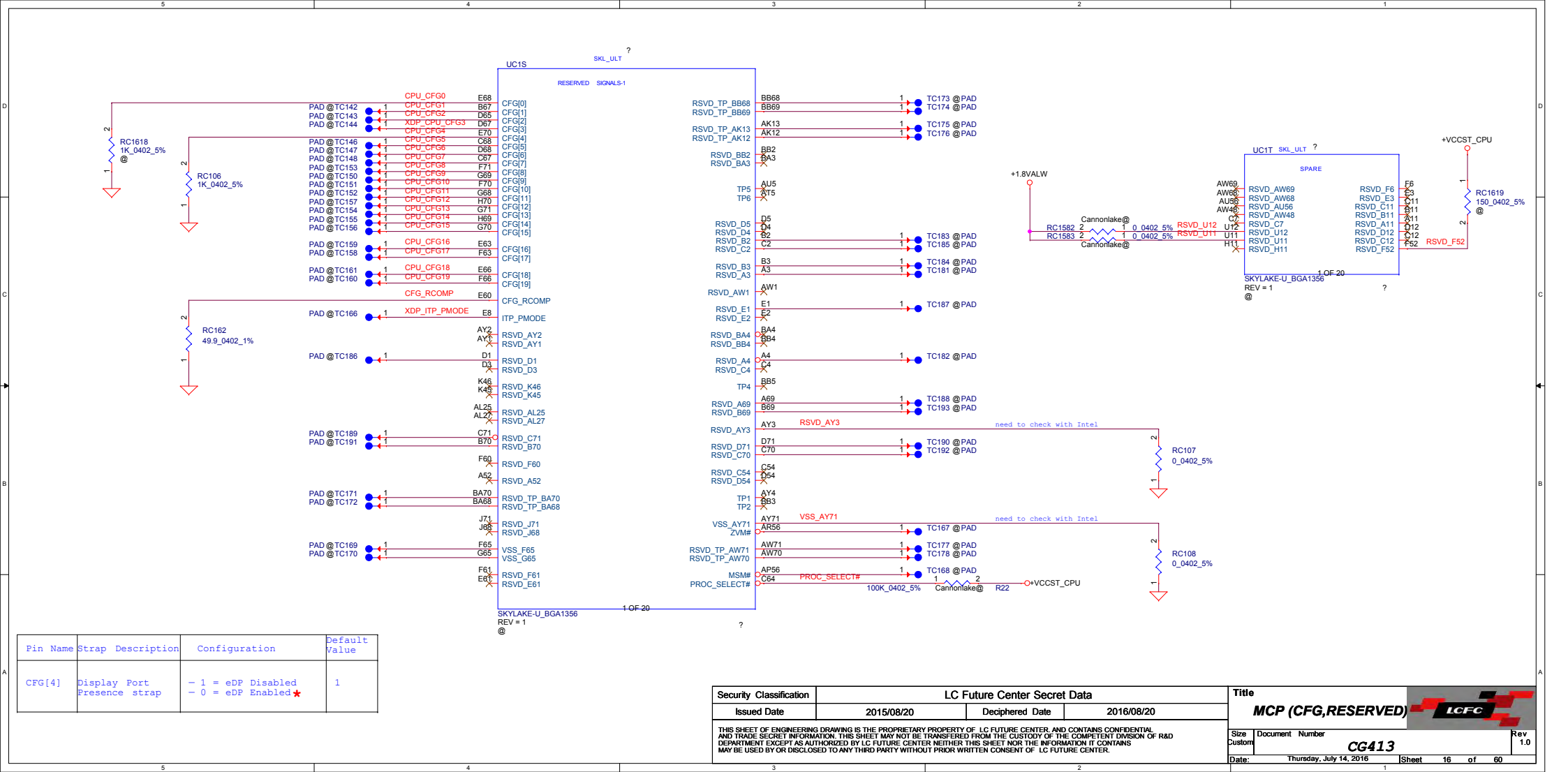
when single end external clock generator used, this pin should be grounded

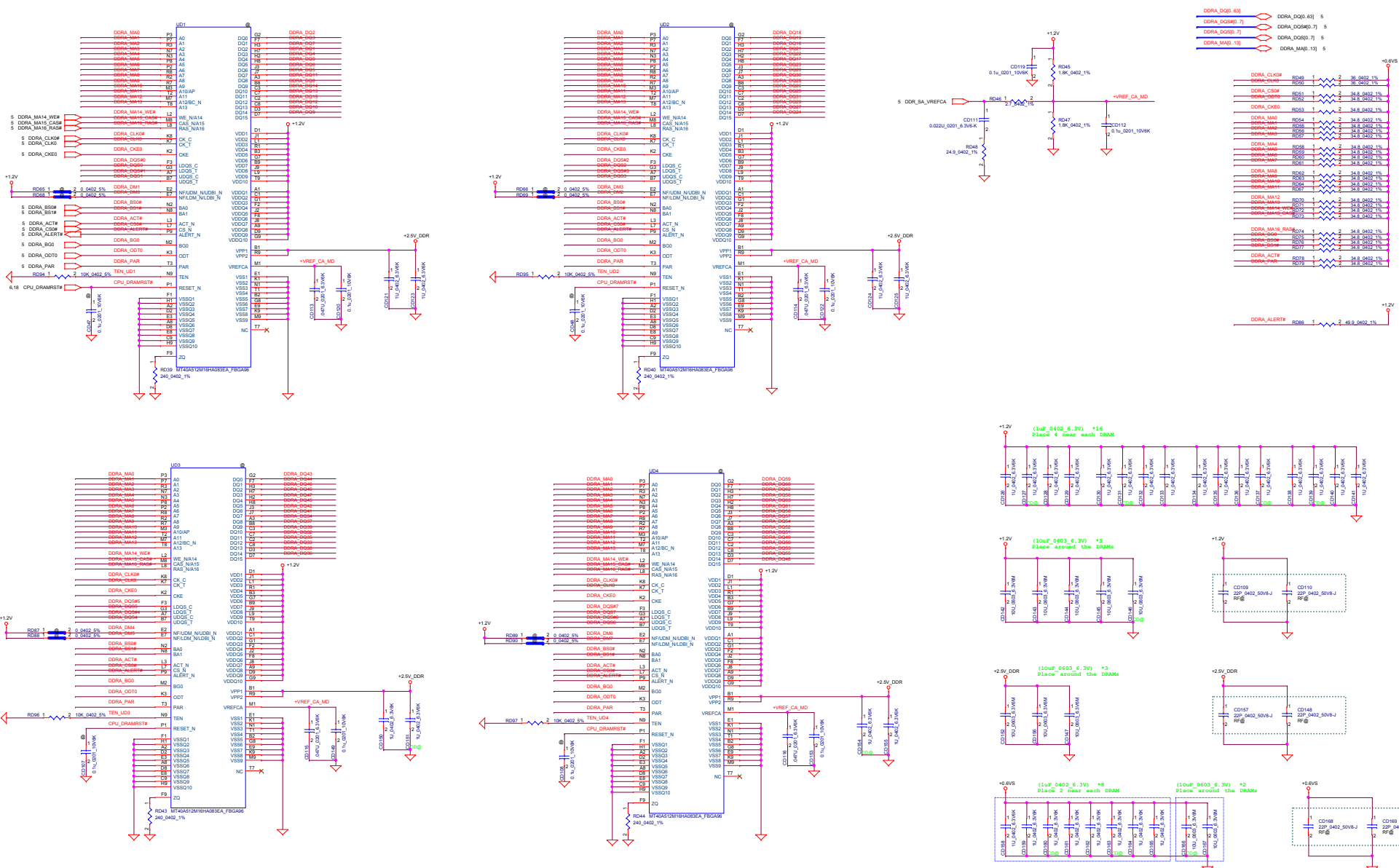




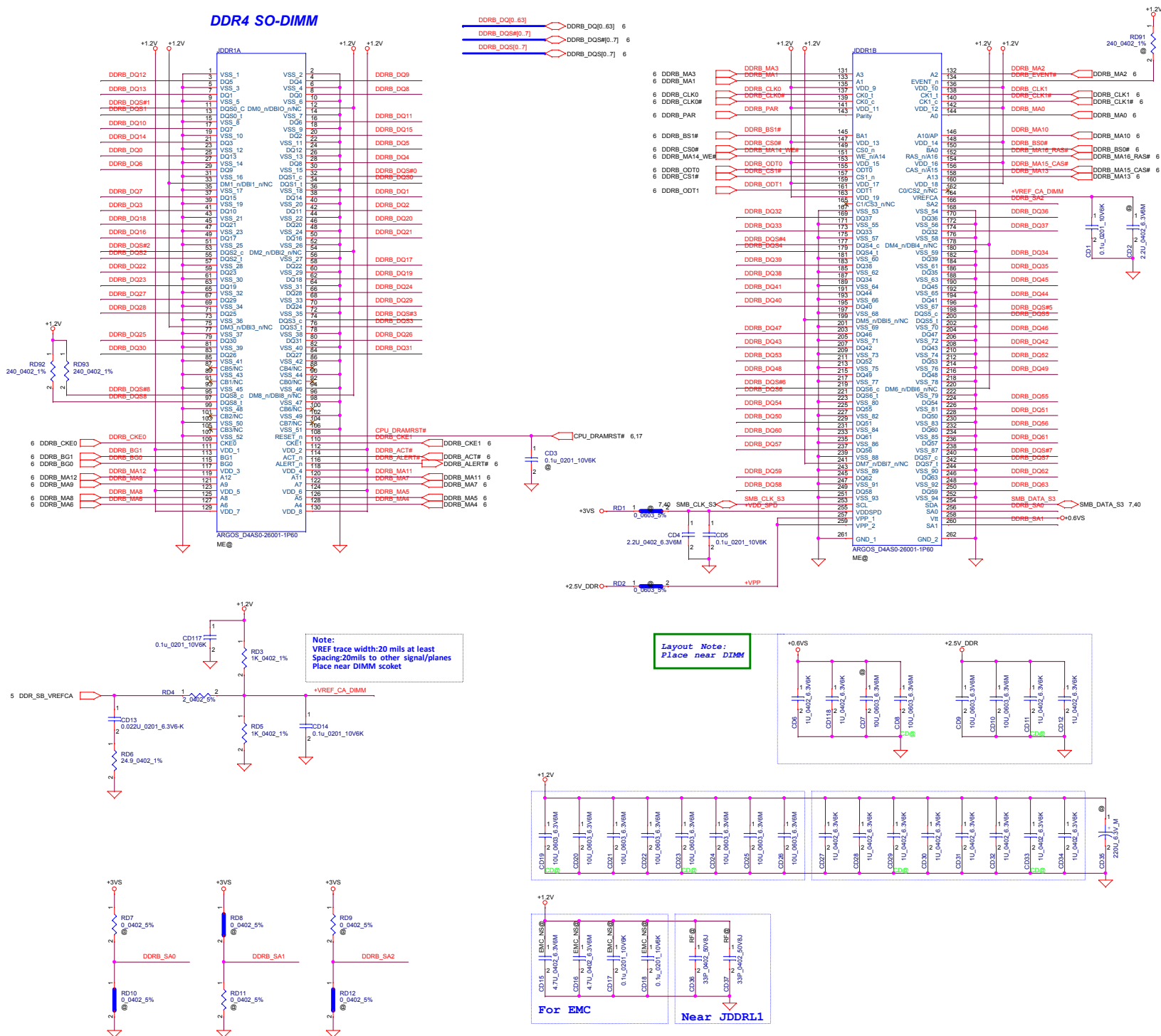


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DDR4 SO-DIMM



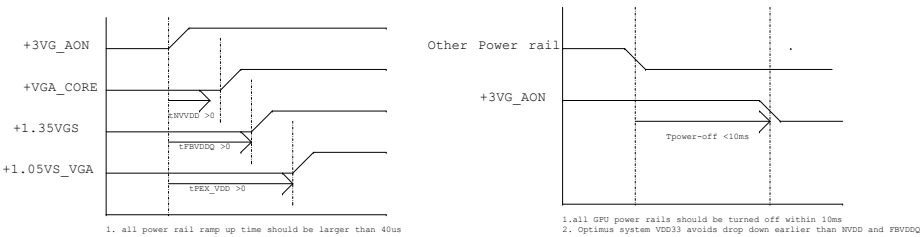
SPD Address = 2H

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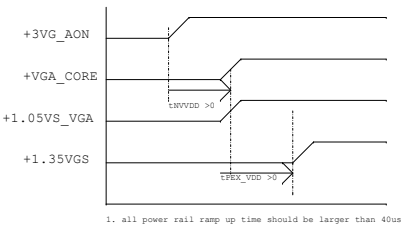
N15x GPIO

GPIO	I/O	ACTIVE	Function Description
GPIO0	OUT	-	FB Enable for GC6 2.0
GPIO1	OUT	N/A	
GPIO2	OUT	N/A	
GPIO3	OUT	N/A	
GPIO4	OUT	N/A	
GPIO5	OUT	N/A	GPU power sequencing---3V3_MAIN_EN
GPIO6	IN	-	GPU wake signal for GC6 2.0
GPIO7	OUT	N/A	
GPIO8	I/O	-	System side PCIe reset Monitor
GPIO9	I/O	N/A	2.2K Pull-up
GPIO10	OUT	N/A	
GPIO11	OUT	-	GPU Core VDD PWM control signal
GPIO12	IN		AC Power Detect Input (10K pull High)
GPIO13	OUT	-	Phase Shedding
GPIO14	IN	N/A	
GPIO15	IN	N/A	
GPIO16		N/A	
GPIO17	IN	N/A	
GPIO18	IN	N/A	
GPIO19	IN	N/A	
GPIO20		N/A	
GPIO21	OUT		GPU PCIe self-reset control
OVERT	OUT		Active Low Thermal Catastrophic Over Temperature

N15V-GM Power Sequence



N15S-GT Power Sequence



Performance Mode P0 TDP at Tj = 102 C* (DDR3)

Products	GPU (4)	Mem (1,5)	NVCLK /MCLK	NVVDD			FBVDD (1.35V)		FBVDDQ (GPU+Mem) (1.35V)		PCI Express (1.05V) (6)		I/O and PLLVDD (1.05V)		Other (3.3V)	
	(W)	(W)	(MHz)	(V)	(A)	(W)	(A)	(W)	(A)	(W)	(mA)	(W)	(mA)	(W)	(mA)	(W)
N14X 128bit 2GB DDR3	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD

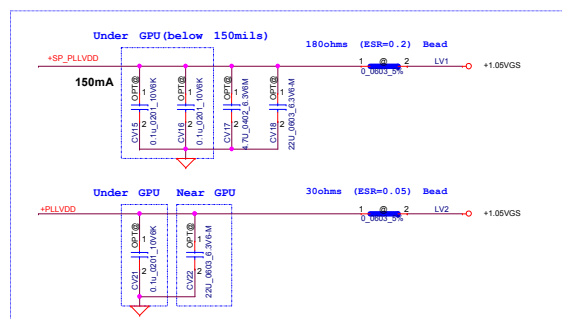
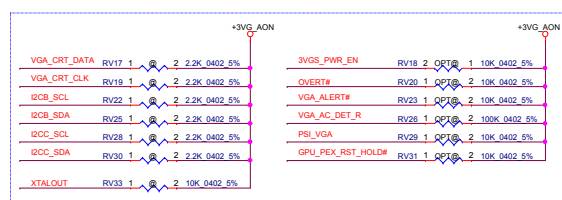
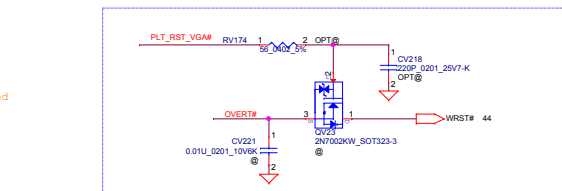
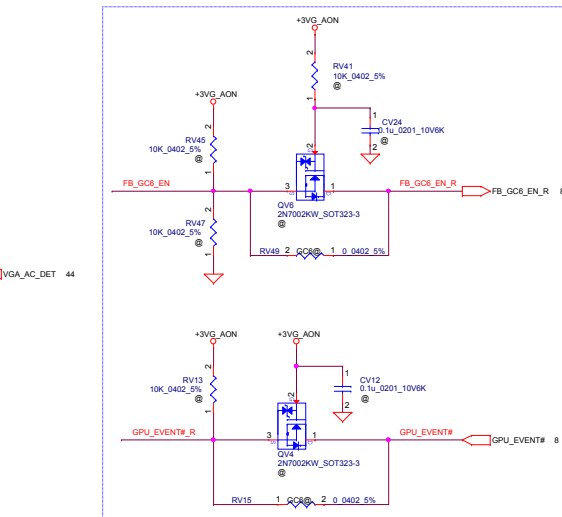
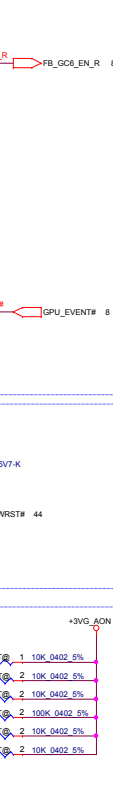
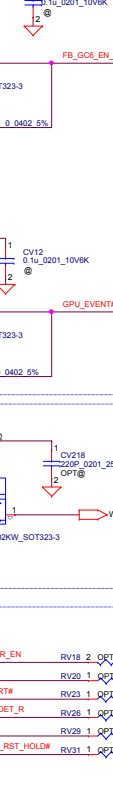
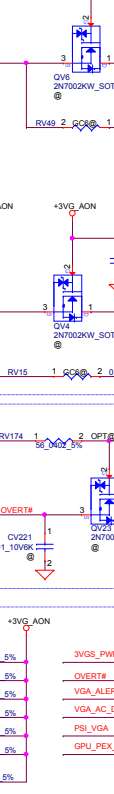
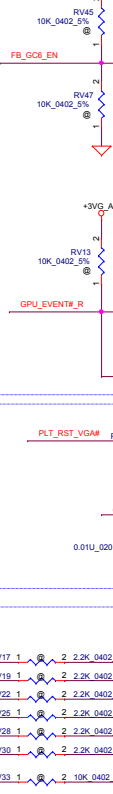
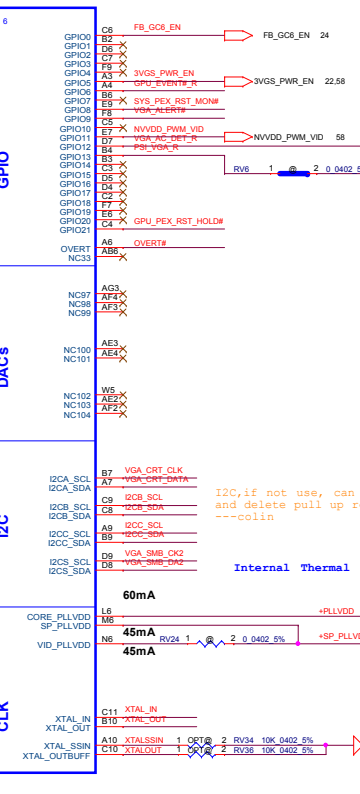
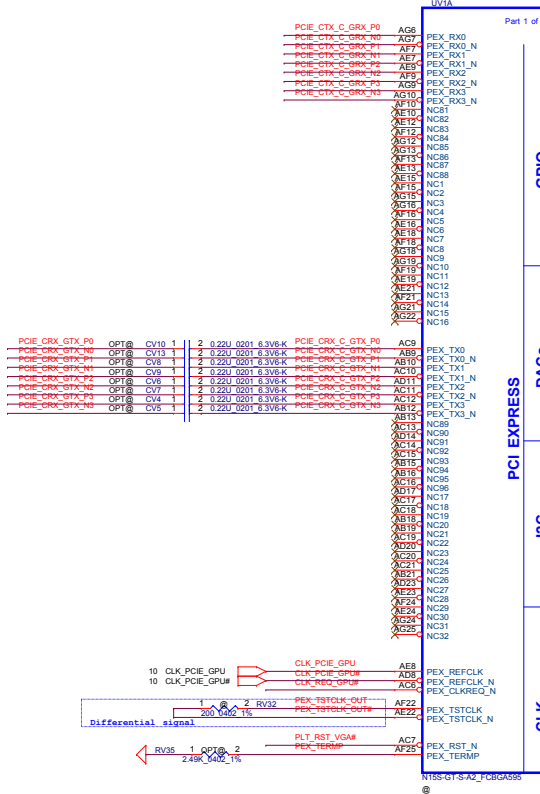
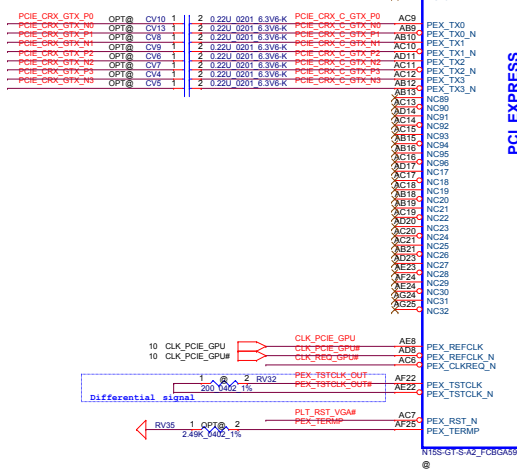
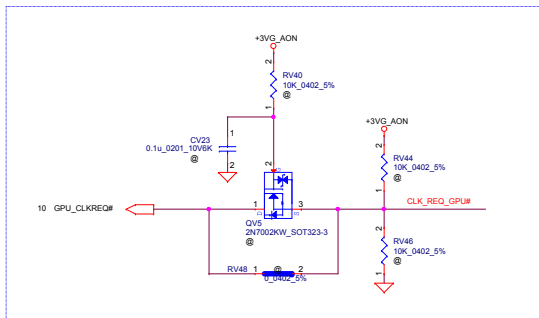
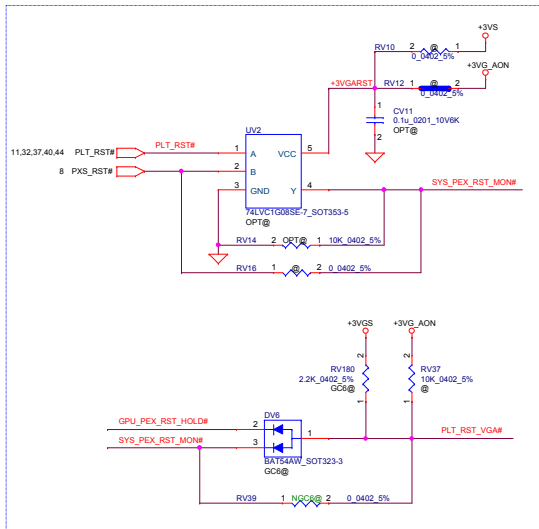
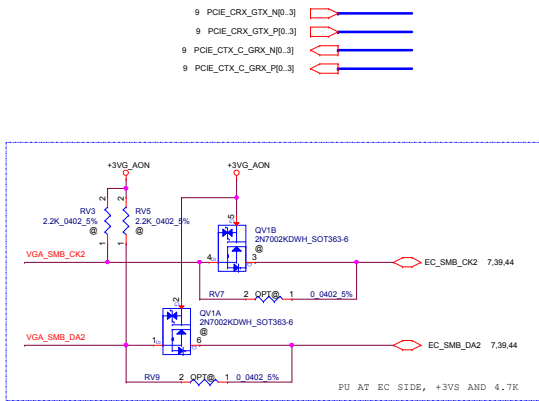
N15x Multi-level Straps

Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VGS	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SI	+3VGS	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VGS	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VGS	Reserved(keep pull-up and pull-down footprint and stuff 50Kohm pull-up)			
STRAP1	+3VGS	Reserved(keep pull-up and pull-down footprint and not stuff by default)			
STRAP2	+3VGS				
STRAP3	+3VGS				
STRAP4	+3VGS				

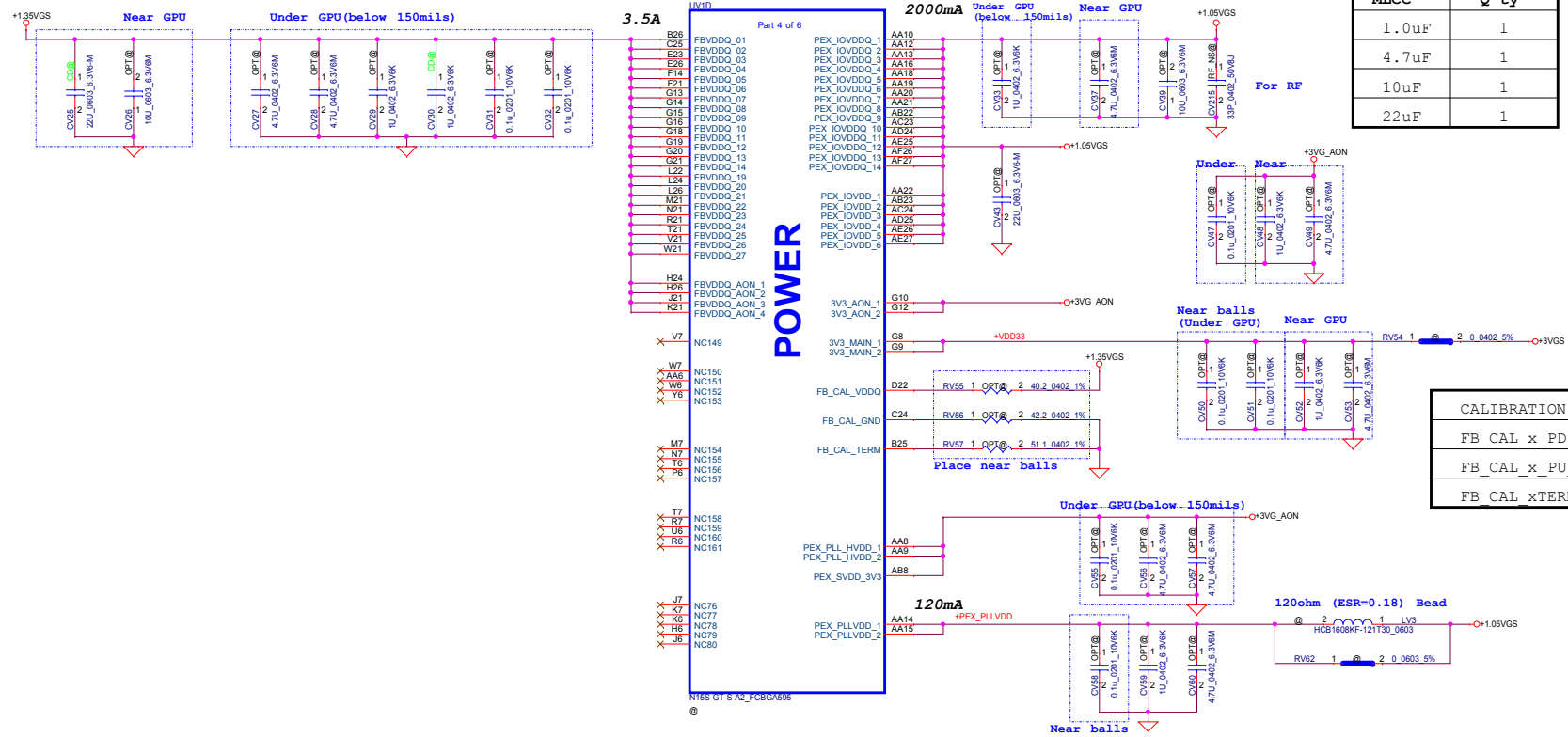
SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

N15x Binary Straps

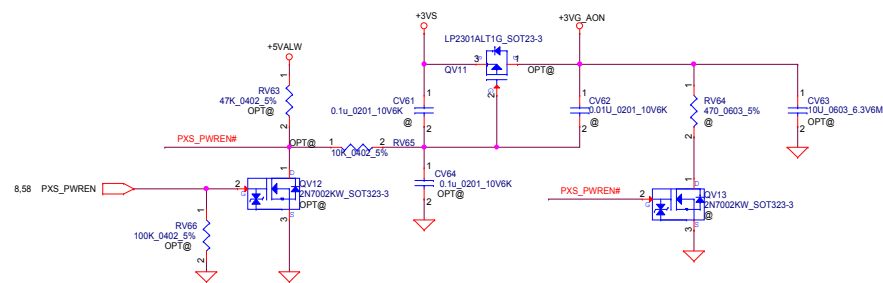
Physical Strapping pin	Power Rail	Strap Mapping
ROM_SCLK	+3VGS	SMB_ALT_ADDR
ROM_SI	+3VGS	SUB_VENDOR
ROM_SO	+3VGS	VGA_DEVICE
STRAP0	+3VGS	RAM_CFG[0]
STRAP1	+3VGS	RAM_CFG[1]
STRAP2	+3VGS	RAM_CFG[2]
STRAP3	+3VGS	RAM_CFG[3]
STRAP4	+3VGS	PCIE_MAX_SPEED



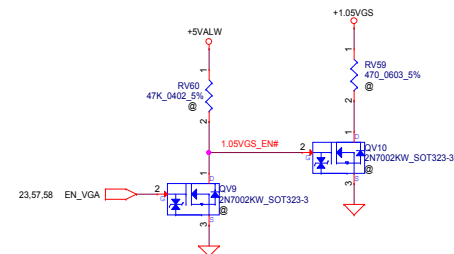
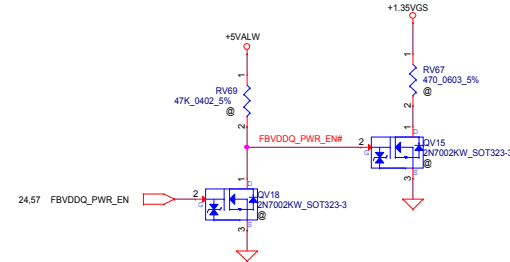
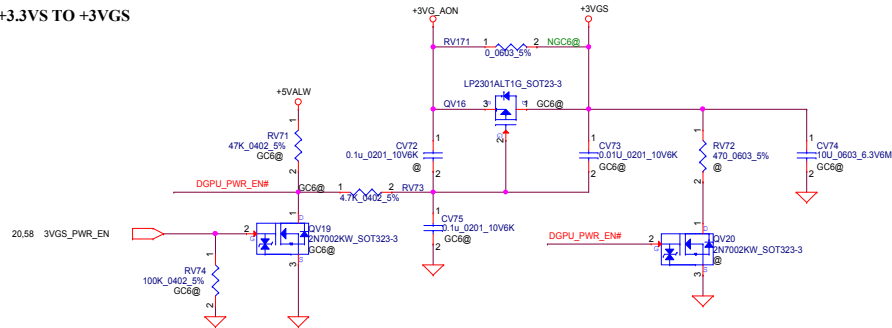
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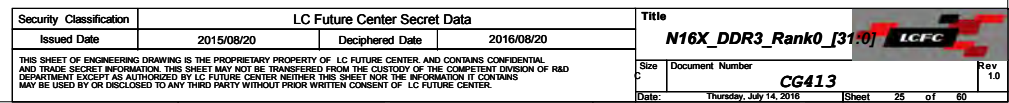
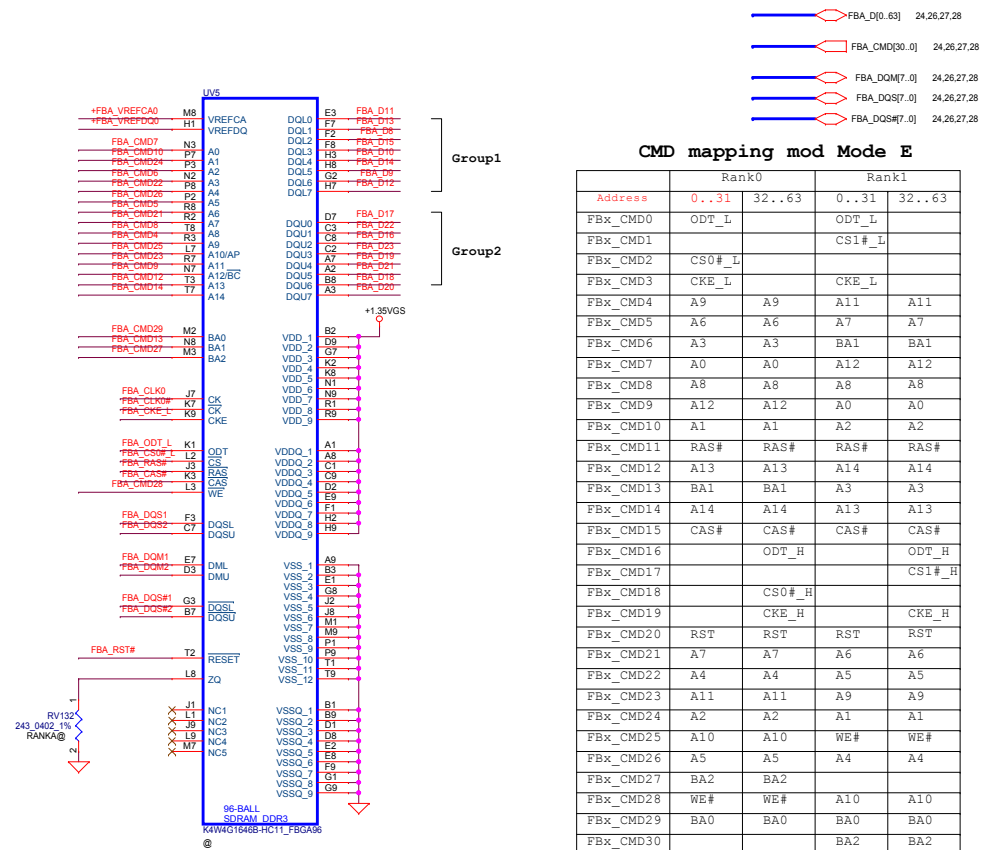
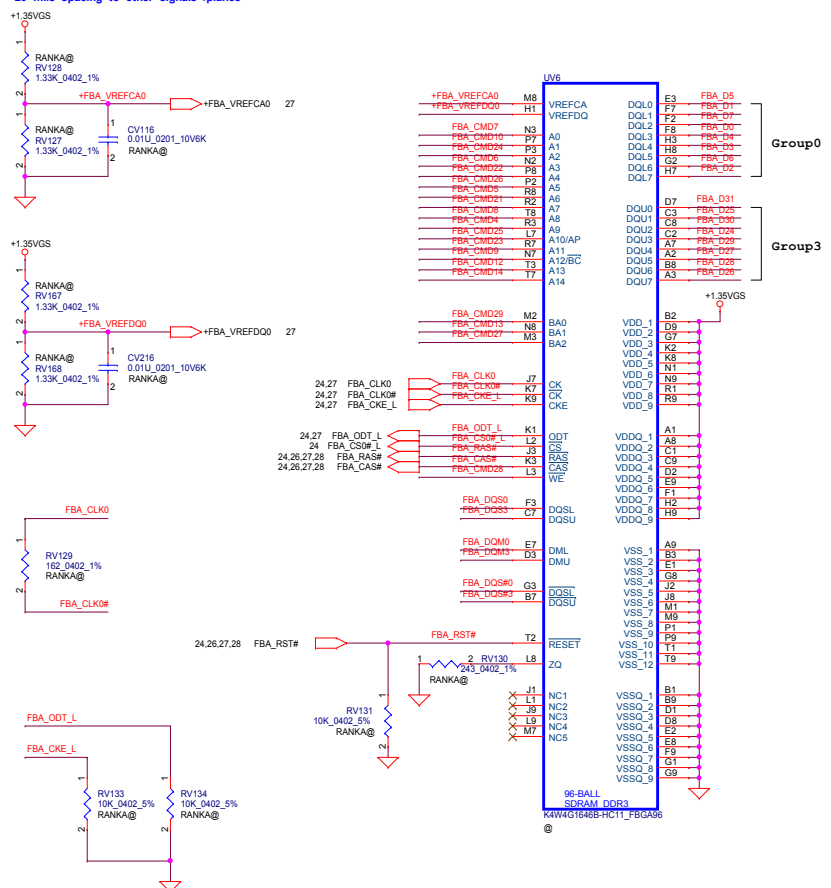


+3.3VS TO +3VG_AON



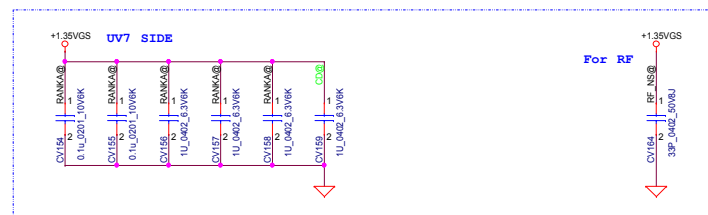
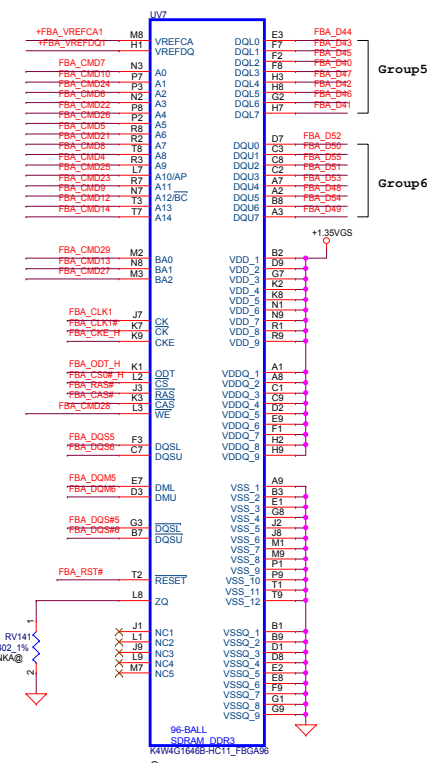
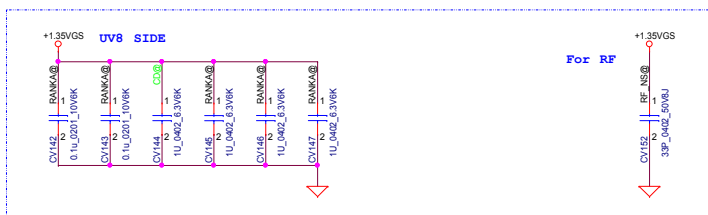
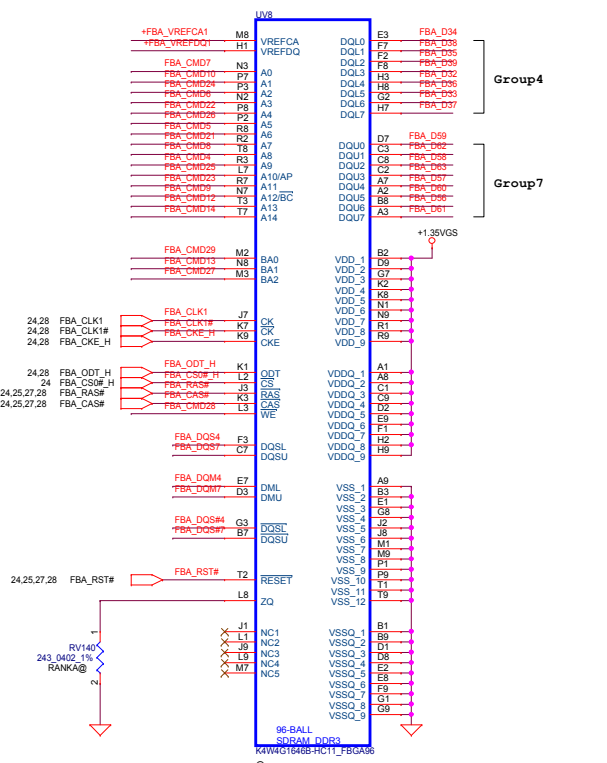
+3.3VS TO +3VGS










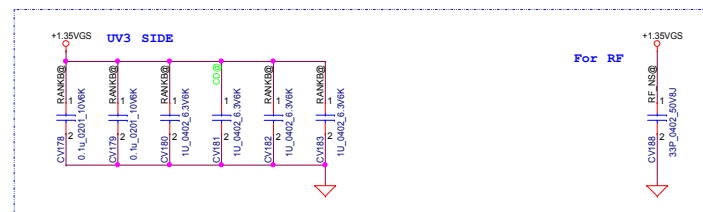
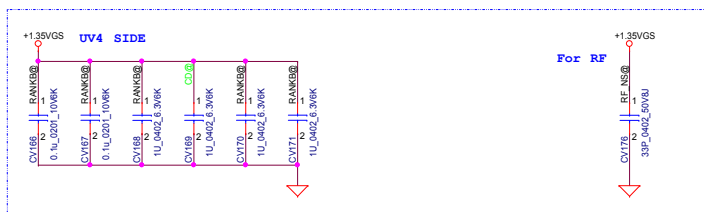
The figure contains three schematic diagrams:

- Top Diagram:** Shows the FBA_VREF pin. It is connected to +1.35VGS through a resistor network consisting of RV135 (1.33K_0402_1%), RV136 (1.33K_0402_1%), and RV137 (1.33K_0402_1%). A capacitor CV141 (0.01u_0201_10V6K) is connected between the node after RV136 and the FBA_VREF pin. The FBA_VREF pin is also connected to FBA_VREFDQ1.
- Middle Diagram:** Shows the FBA_VREFDQ1 pin. It is connected to +1.35VGS through a resistor network consisting of RV169 (1.33K_0402_1%), RV170 (1.33K_0402_1%), and RV171 (1.33K_0402_1%). A capacitor CV217 (0.01u_0201_10V6K) is connected between the node after RV169 and the FBA_VREFDQ1 pin. The FBA_VREFDQ1 pin is also connected to FBA_VREFDQ1.
- Bottom Diagram:** Shows the FBA_CLK1# pin. It is connected to FBA_CLK1 through a resistor RV137 (162_0402_1%).

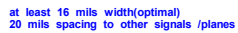


	FBA_D[0..63]	24,25,27,28
	FBA_CMD[30..0]	24,25,27,28
	FBA_DOM[7..0]	24,25,27,28
	FBA_DQS[7..0]	24,25,27,28
	FBA_DQS#[7..0]	24,25,27,28

	Rank0		Rank1	
Address	0..31	32..63	0..31	32..63
FBx_CMD0	ODT_L		ODT_L	
FBx_CMD1			CS1#_L	
FBx_CMD2	CS0#_L			
FBx_CMD3	CKE_L		CKE_L	
FBx_CMD4	A9	A9	A11	A11
FBx_CMD5	A6	A6	A7	A7
FBx_CMD6	A3	A3	BA1	BA1
FBx_CMD7	A0	A0	A12	A12
FBx_CMD8	A8	A8	A8	A8
FBx_CMD9	A12	A12	A0	A0
FBx_CMD10	A1	A1	A2	A2
FBx_CMD11	RAS#	RAS#	RAS#	RAS#
FBx_CMD12	A13	A13	A14	A14
FBx_CMD13	BA1	BA1	A3	A3
FBx_CMD14	A14	A14	A13	A13
FBx_CMD15	CAS#	CAS#	CAS#	CAS#
FBx_CMD16		ODT_H		ODT_H
FBx_CMD17			CS1#_H	
FBx_CMD18		CS0#_H		
FBx_CMD19		CKE_H		CKE_H
FBx_CMD20	RST	RST	RST	RST
FBx_CMD21	A7	A7	A6	A6
FBx_CMD22	A4	A4	A5	A5
FBx_CMD23	A11	A11	A9	A9
FBx_CMD24	A2	A2	A1	A1
FBx_CMD25	A10	A10	WE#	WE#
FBx_CMD26	A5	A5	A4	A4
FBx_CMD27	BA2	BA2		
FBx_CMD28	WE#	WE#	A10	A10
FBx_CMD29	BA0	BA0	BA0	BA0
FBx_CMD30			BA2	BA2

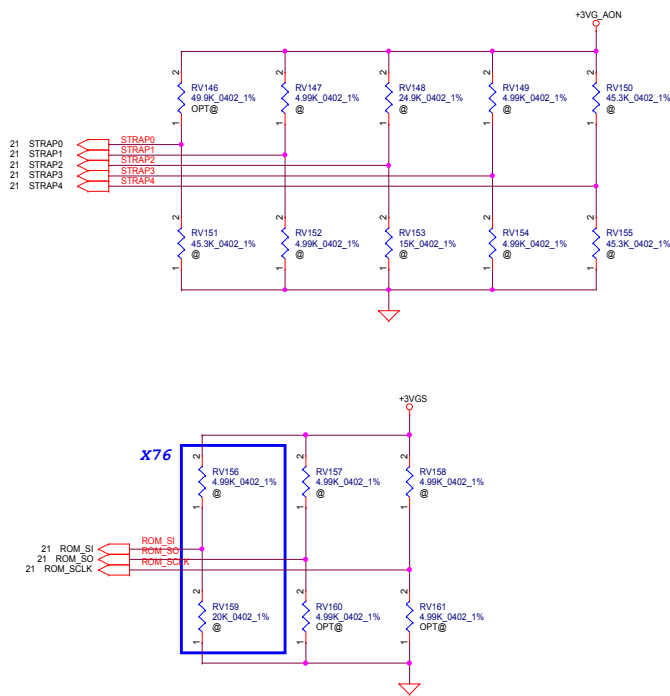


CMD mapping mod Mode E				
	Rank0		Rank1	
Address	0..31	32..63	0..31	32..63
FbX_CMD0	ODT_L		ODT_L	
FbX_CMD1			CS1#_L	
FbX_CMD2	CS0#_L			
FbX_CMD3	CKE_L		CKE_L	
FbX_CMD4	A9	A9	A11	A11
FbX_CMD5	A6	A6	A7	A7
FbX_CMD6	A3	A3	BA1	BA1
FbX_CMD7	A0	A0	A12	A12
FbX_CMD8	A8	A8	A8	A8
FbX_CMD9	A12	A12	A0	A0
FbX_CMD10	A1	A1	A2	A2
FbX_CMD11	RAS#	RAS#	RAS#	RAS#
FbX_CMD12	A13	A13	A14	A14
FbX_CMD13	BA1	BA1	A3	A3
FbX_CMD14	A14	A14	A13	A13
FbX_CMD15	CAS#	CAS#	CAS#	CAS#
FbX_CMD16		ODT_H		ODT_H
FbX_CMD17				CS1#_H
FbX_CMD18		CS0#_H		
FbX_CMD19		CKE_H		CKE_H
FbX_CMD20	RST	RST	RST	RST
FbX_CMD21	A7	A7	A6	A6
FbX_CMD22	A4	A4	A5	A5
FbX_CMD23	A11	A11	A9	A9
FbX_CMD24	A2	A2	A1	A1
FbX_CMD25	A10	A10	WE#	WE#
FbX_CMD26	A5	A5	A4	A4
FbX_CMD27	BA2	BA2		
FbX_CMD28	WE#	WE#	A10	A10
FbX_CMD29	BA0	BA0	BA0	BA0
FbX_CMD30			BA2	BA2



For RF





Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VGS	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SI	+3VGS	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VGS	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VGS	Reserved(keep pull-up and pull-down footprint and stuff 50Kohm pull-up)			
STRAP1	+3VGS	Reserved(keep pull-up and pull-down footprint and not stuff by default)			
STRAP2	+3VGS				
STRAP3	+3VGS				
STRAP4	+3VGS				

Resistor Values	Pull-up to +3VGS	Pull-down to Gnd
4.99K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
24.9K	1100	0100
30.1K	1101	0101
34.8K	1110	0110
45.3K	1111	0111

DEVID_SEL	
0	(Default)
1	

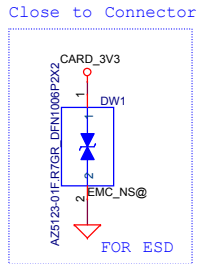
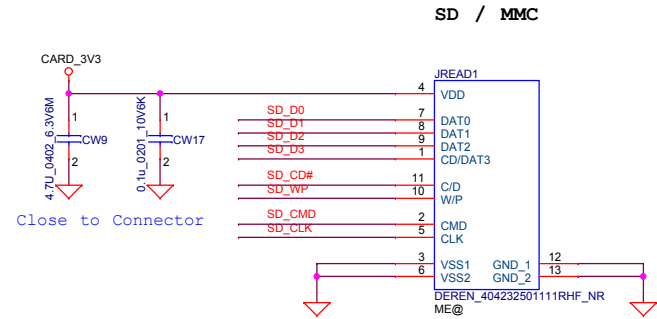
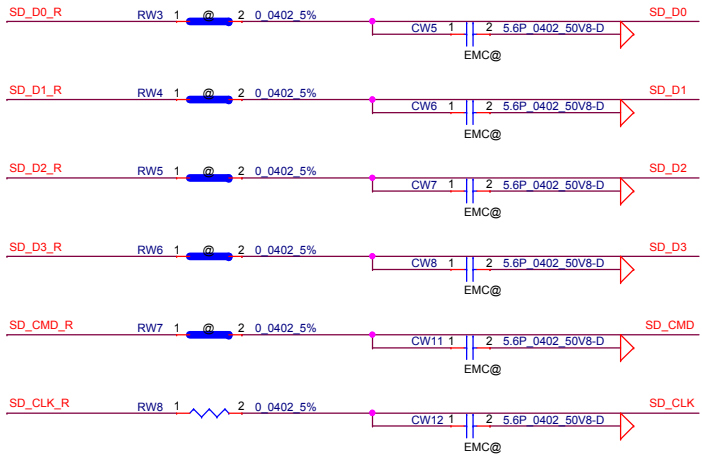
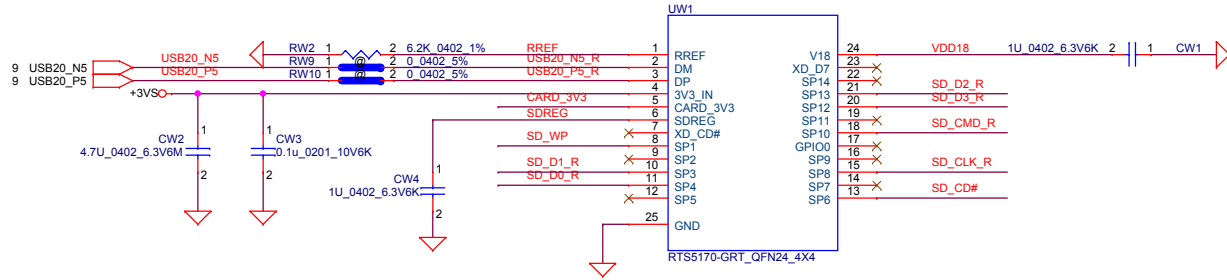
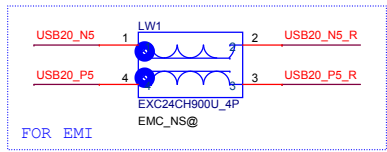
PCIE_CFG	
0	(Default)
1	



SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

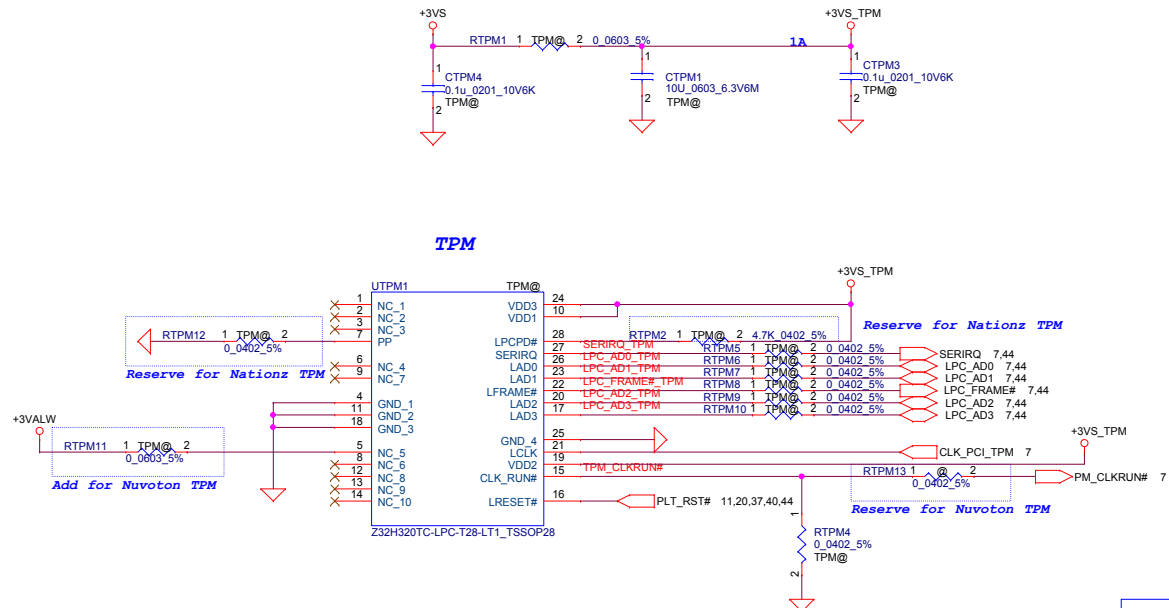
VGA_DEVICE	
0	3D Device (Class Code 302h)
1	VGA Device (Default)

GPU	Configuration	FB Memory (DDR3L)		ROM_SI	ROM_SO	ROM_SCLK	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4
N16S-GTR N16V-GMR1	Single-Rank	Samsung 900MHz	K4W4G1646E-BC1A	0x1	PD 4.99K	PD 4.99K	PU 49.9K	Un-stuff	Un-stuff	Un-stuff	Un-stuff
			256M x 16	PD 10K							
		Hynix 900MHz	H5TC4G63CFR-N0C	0x2							
			256M x 16	PD 15K							
		Micron 900MHz	MT41J256M16LY-091G:N	0x6							
			256M x 16	PD 34.8K							
	Dual-Rank	Samsung 900MHz	K4W4G1646E-BC1A	0xF							
			256M x 16	PU 45.3K							
		Hynix 900MHz	H5TC4G63CFR-N0C	0xE							
			256M x 16	PU 34.8K							
		Micron 900MHz	MT41J256M16LY-091G:N	0xA							
			256M x 16	PU 15K							

VRAM	X76 P/N	VRAM Q'ty	VRAM P/N
Samsung	X7610212201	4	SA000063F20
	X7610212001	8	
Hynix	X7610212202	4	SA00007DU10
	X7610212101	8	
Micron	X7610212203	4	SA00007QJ00
	N/A	8	



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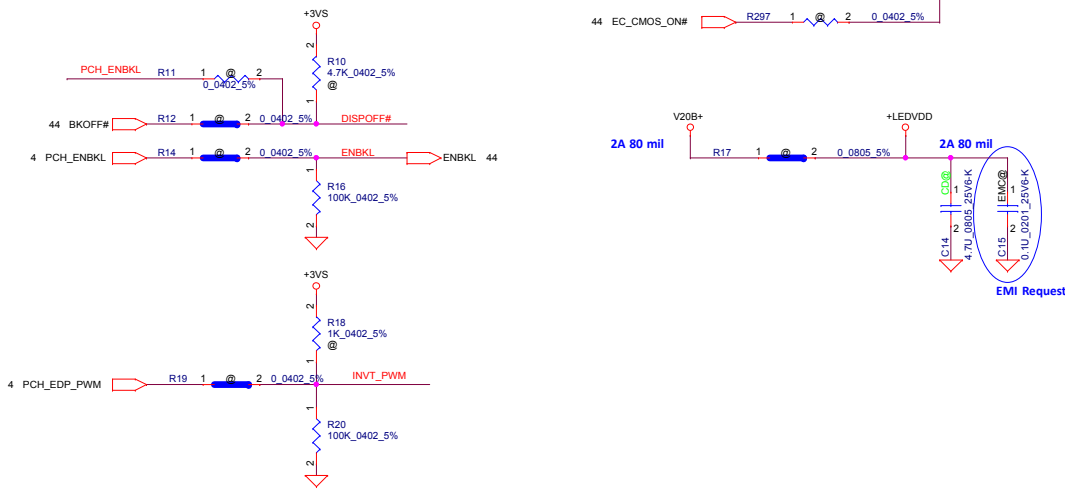
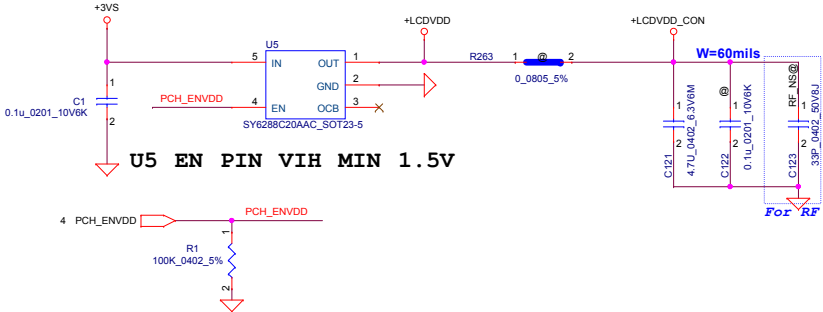
	Nationz TPM	Nuvoton TPM
RTPM2	Stuff	NC
RTPM12	Stuff	NC
RTPM11	NC	Stuff

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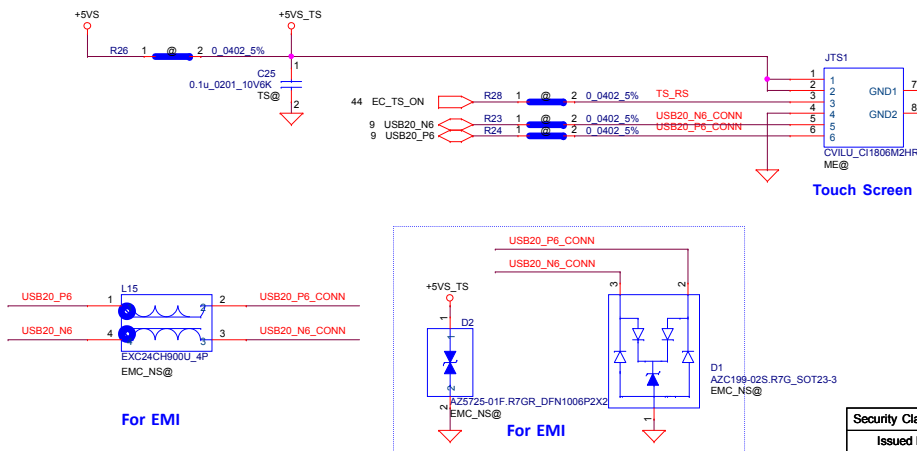
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TPM		
Size	Document	Number
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		Rev 1.0



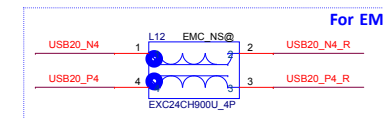
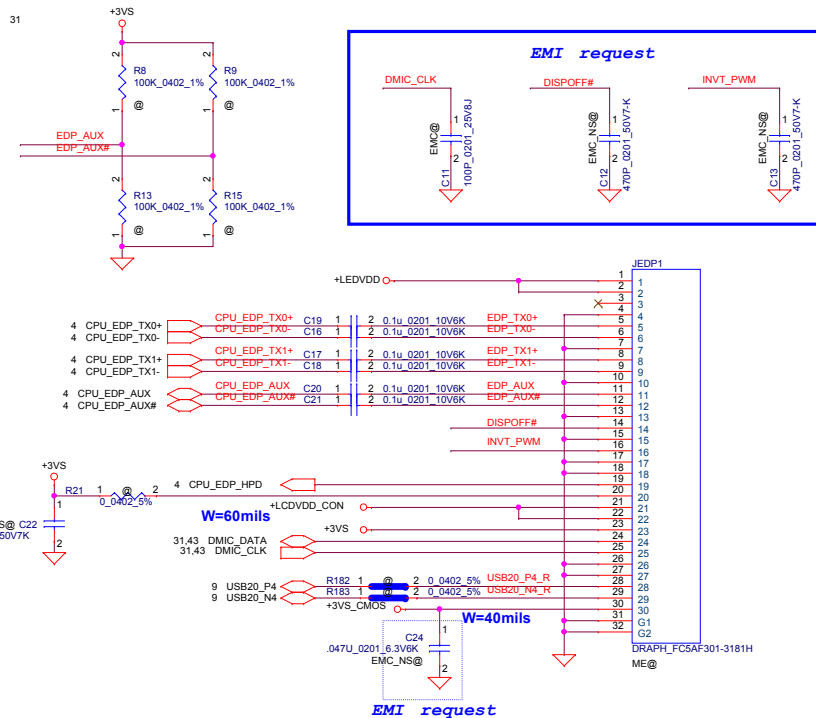
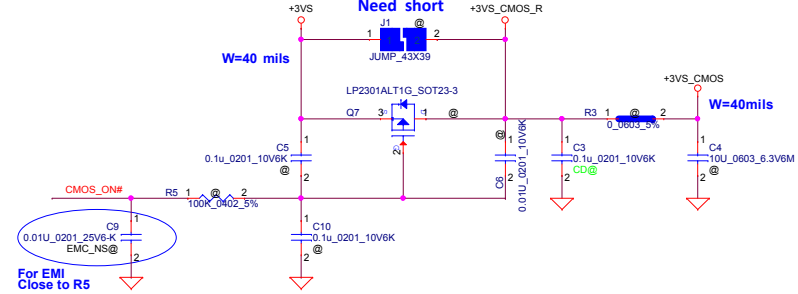
LCD POWER CIRCUIT



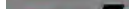
Touch Screen

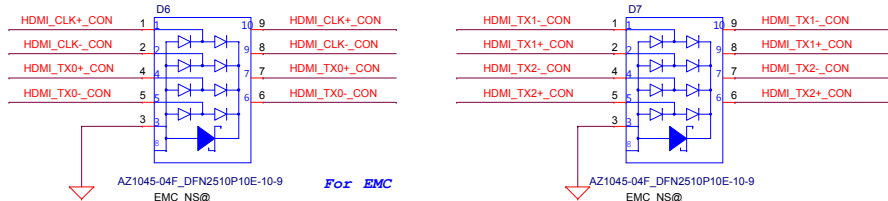
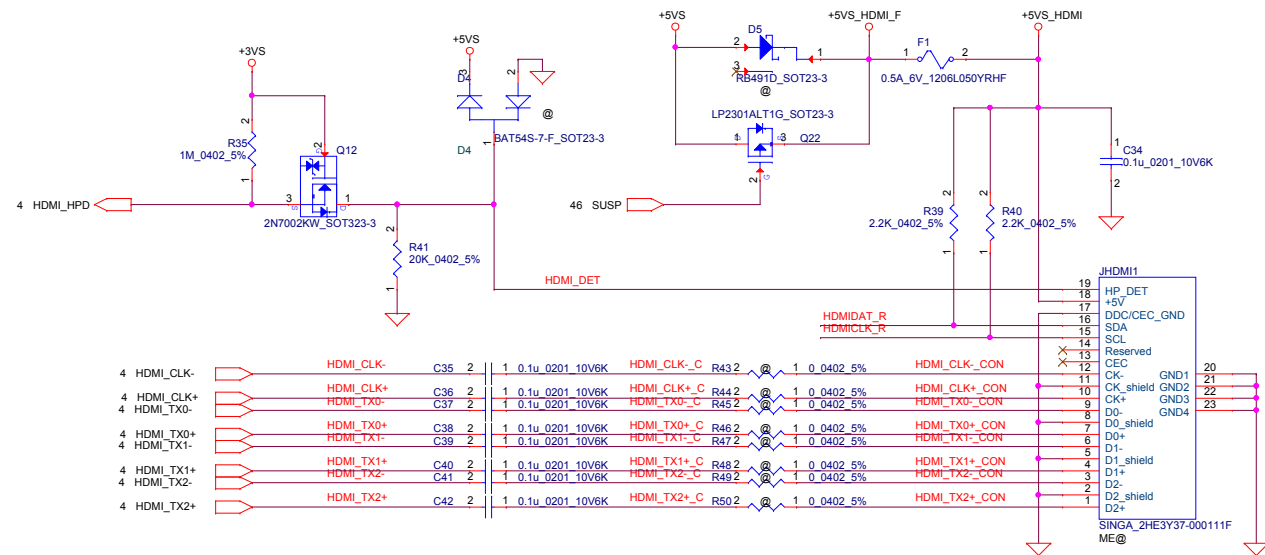
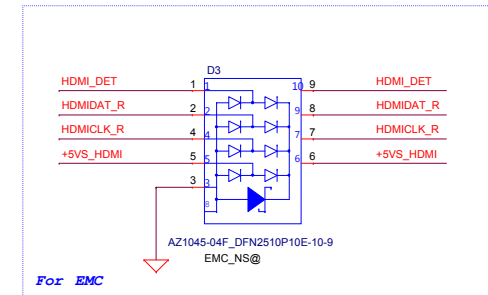


CMOS Camera



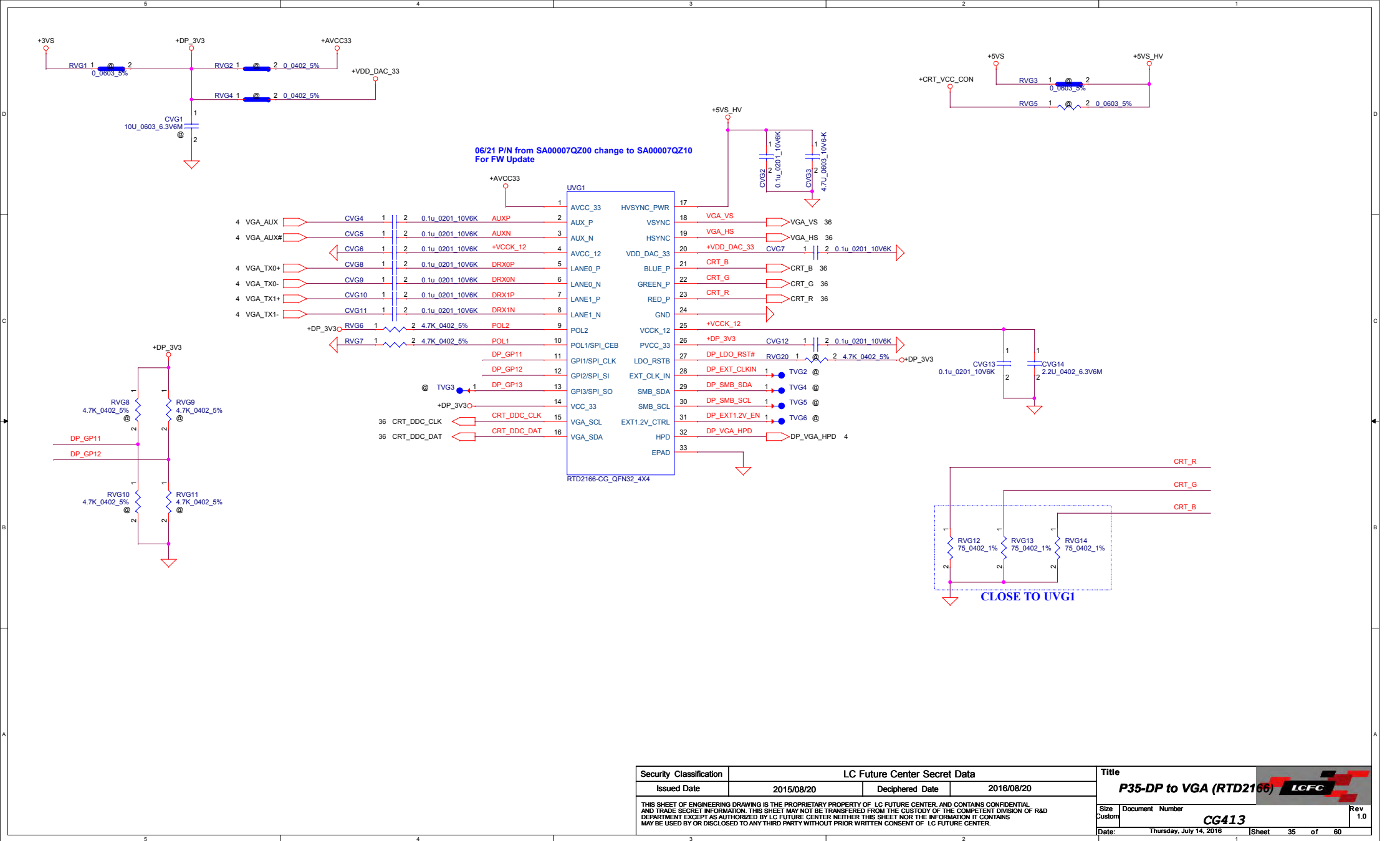
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Title			
eDP/CMOS/Touch screen			
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CG413			
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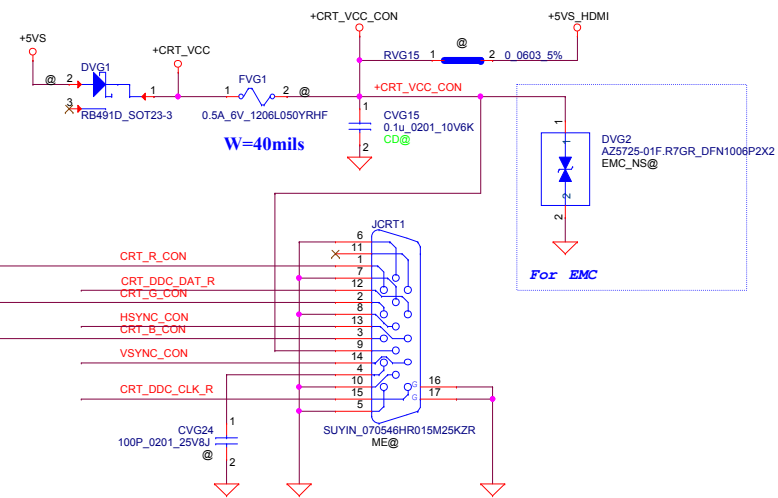
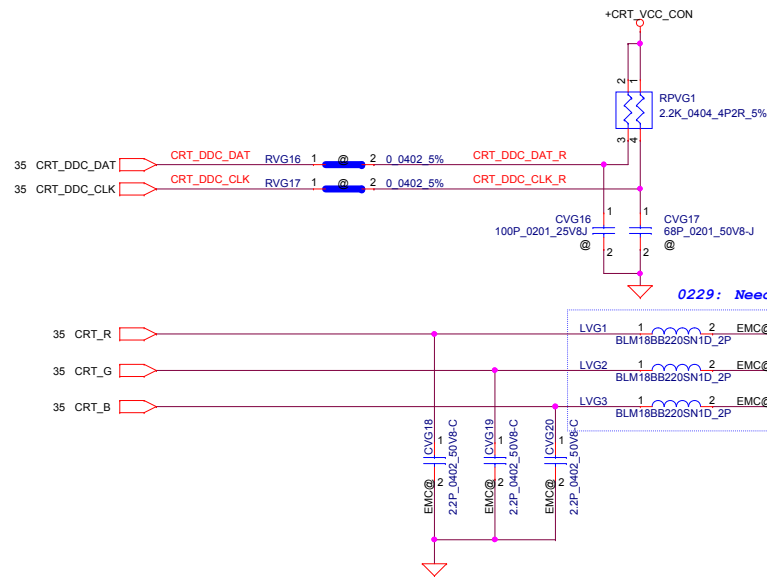
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Title			
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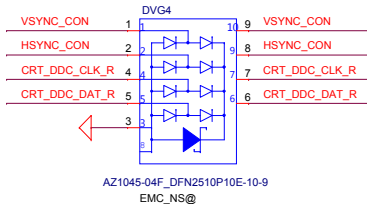
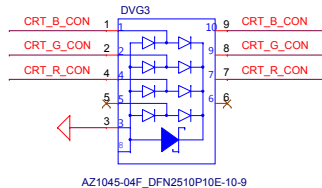
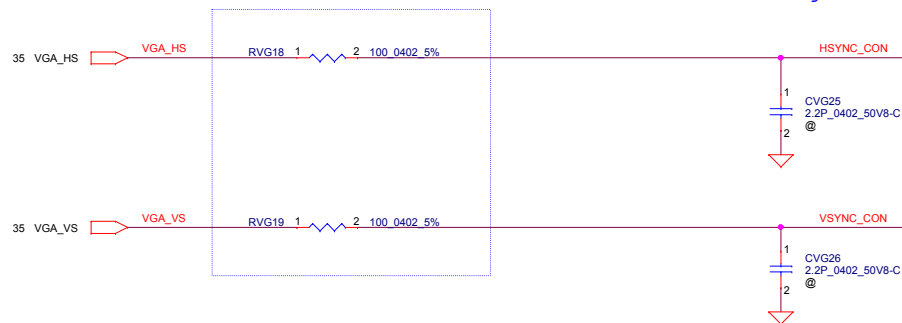



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				Date: Thursday, July 14, 2016	Rev 1.0
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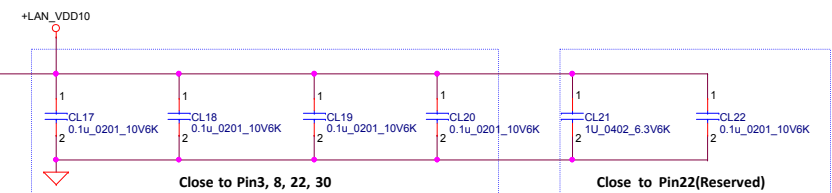
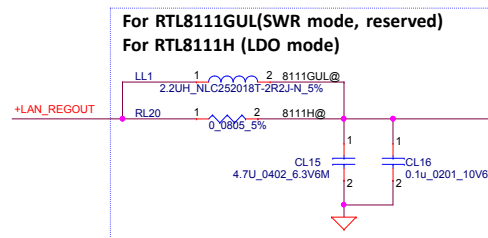
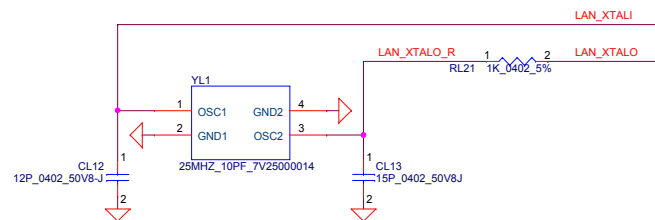
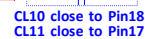
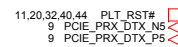
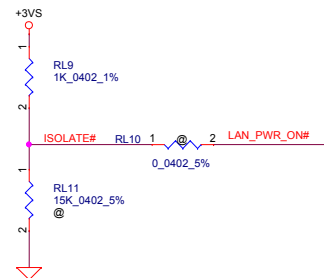
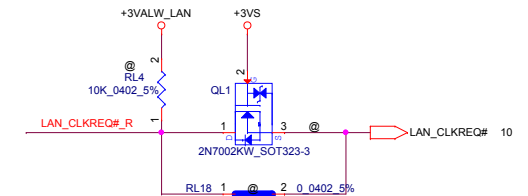
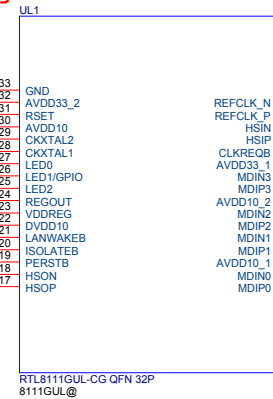
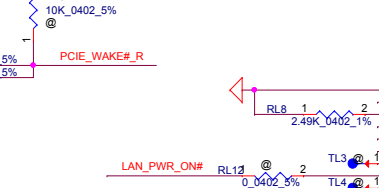
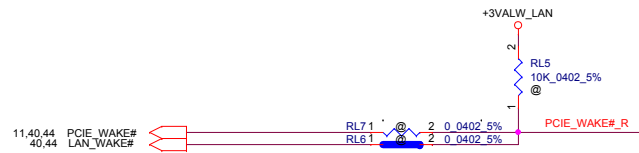
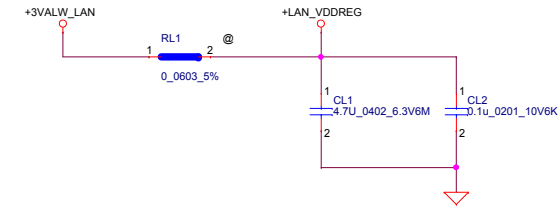
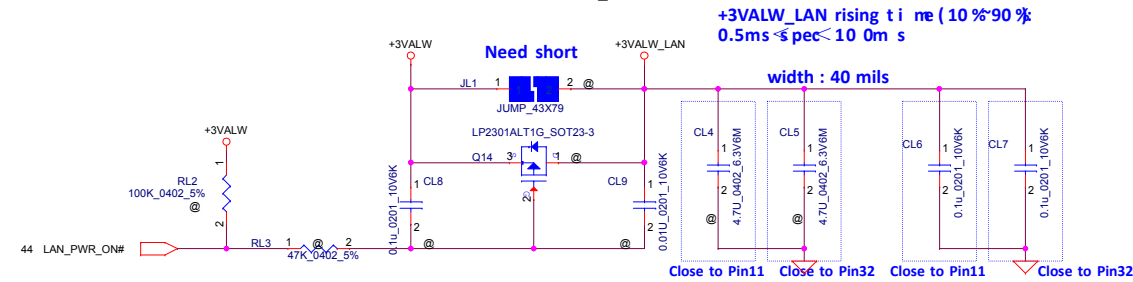
CRT Connector



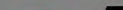
0714: SVT For VGA 20m cable test issue change to 100ohm



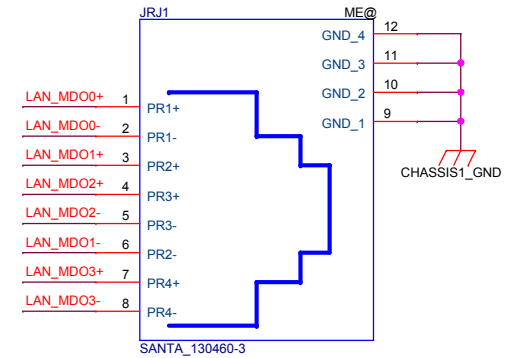
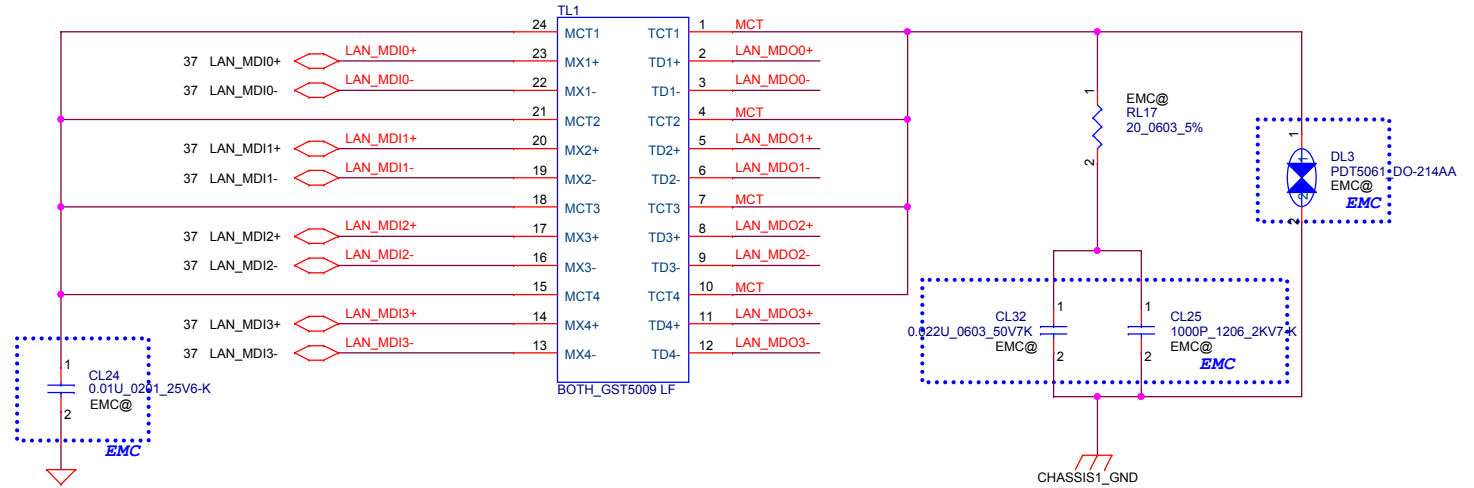
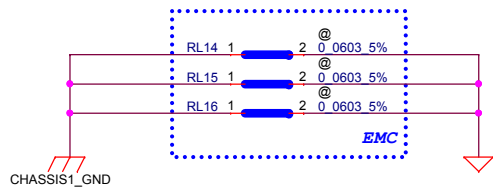
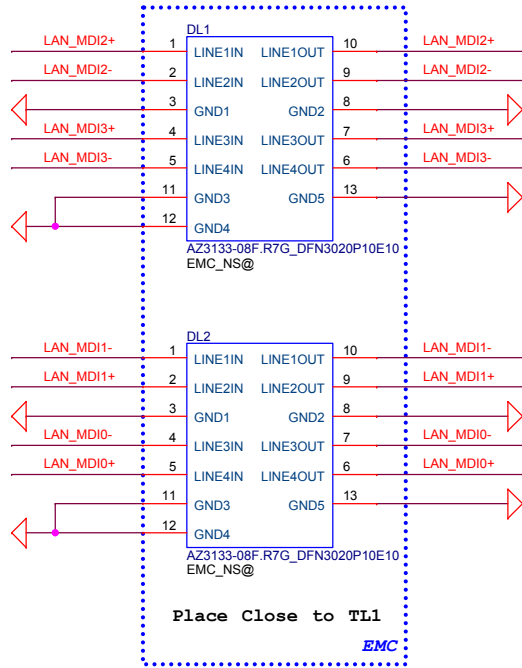
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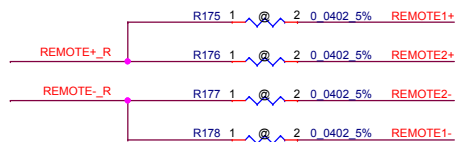
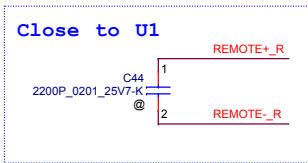
Layout Note: LL1 must be within 200mil to Pin24, CL15,CL16 must be within 200mil to LL1
+LAN_REGOUT: Width =60mil

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DL1/DL2 1'S PN:SC300003M00

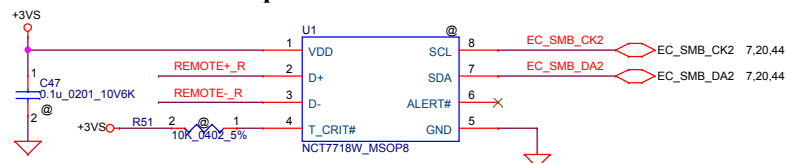


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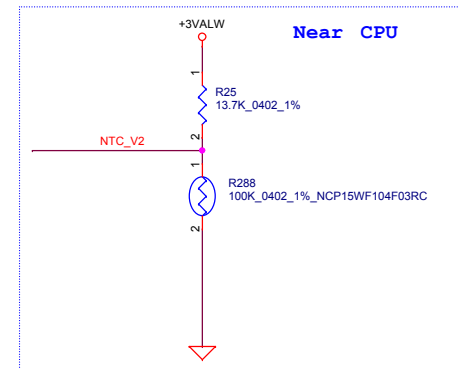
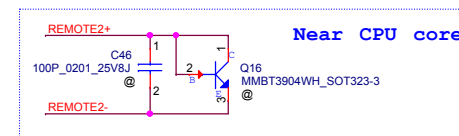
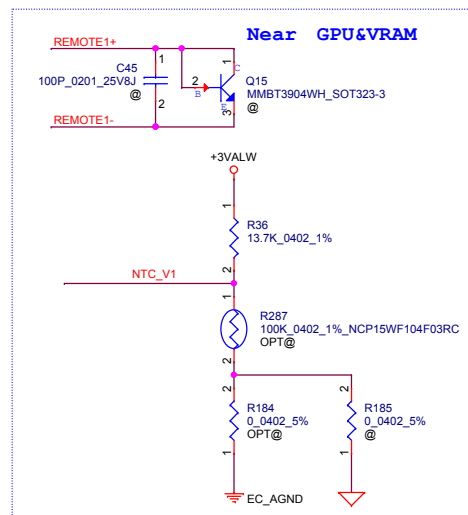


REMOTE+/-_R, REMOTE1+/-, REMOTE2+/-:
Trace width/space:10/10 mil
Trace length:<8"

SMSC thermal sensor placed near DIMM

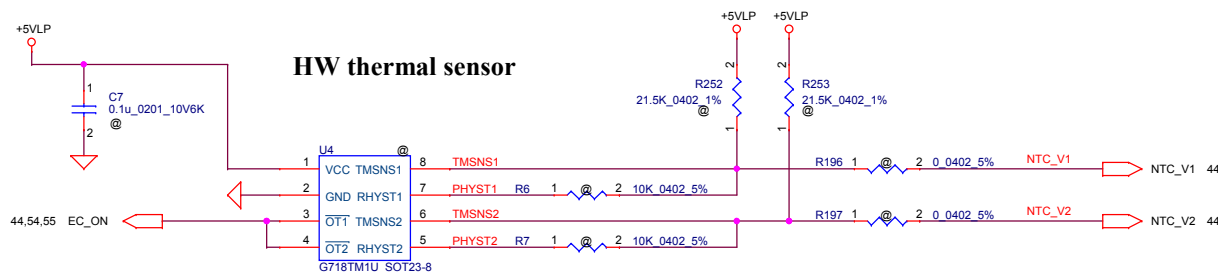


Address 1001_101xb

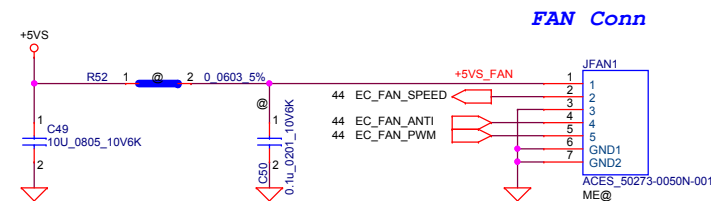


for layout optimized, change the EC_AGND to GND

HW thermal sensor

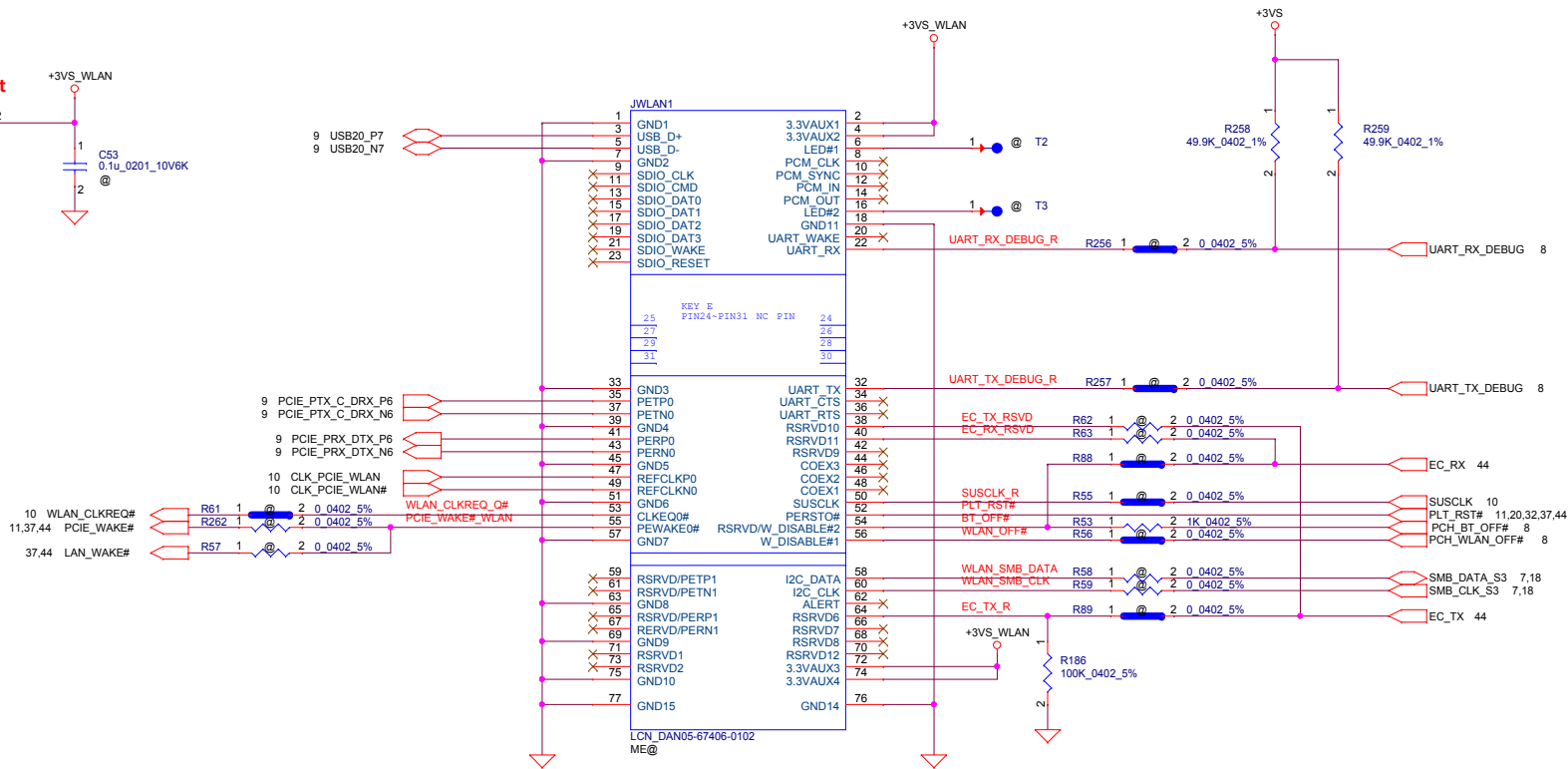



over temperature threshold:
 $RSET=3*RTMH$
 $92+/-30C$
Hysteresis temperature threshold.
 $RHYST=(RSET*RTML)/(3*RTML-RSET)$
 $56+/-30C$



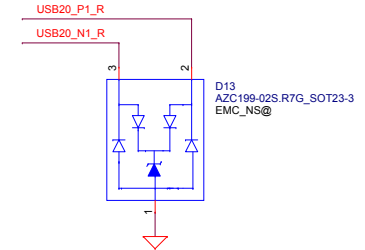
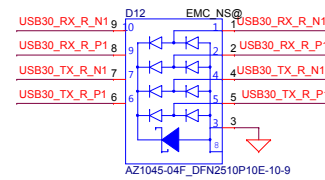
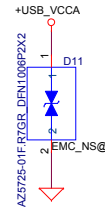
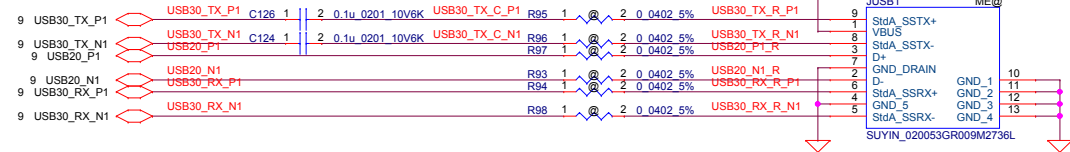
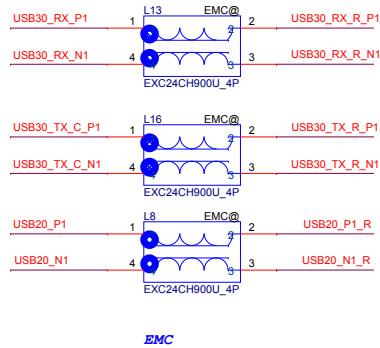
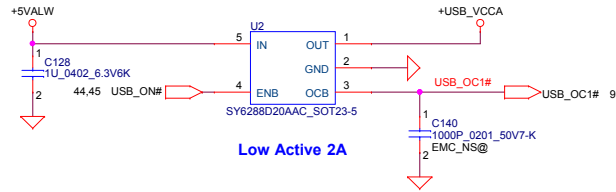
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Issued Date	2015/08/20	Deciphered Date	2016/08/20	Size	Document	Number
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Mini-Express Card(WLAN/WiMAX)

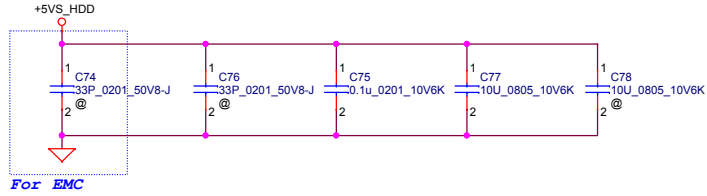
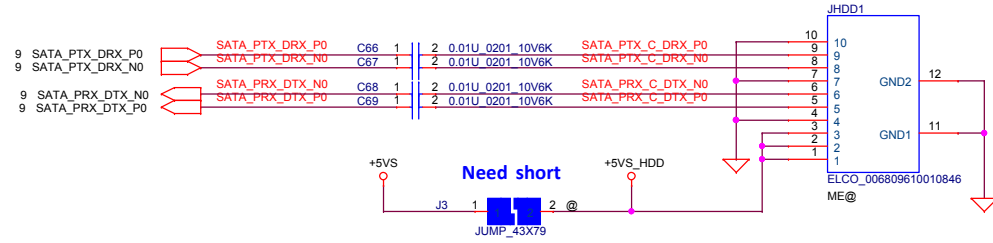


Security Classification		LC Future Center Secret Data		Title		
Issued Date	2015/08/20	Deciphered Date	2016/08/20	NGFF WLAN		
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Date:	Thursday, July 14, 2016		Sheet	40	of	60

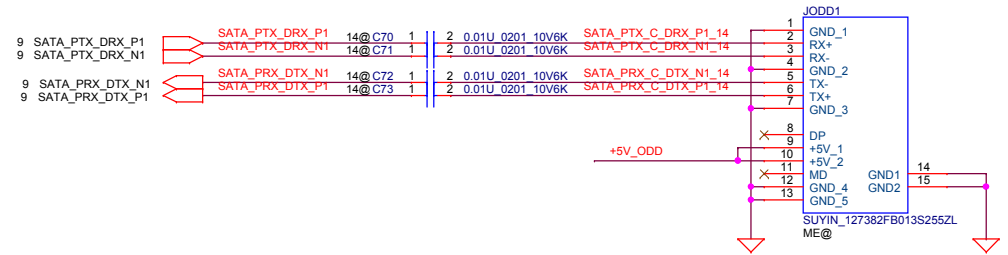
LEFT SIDE USB3.0 PORT x1



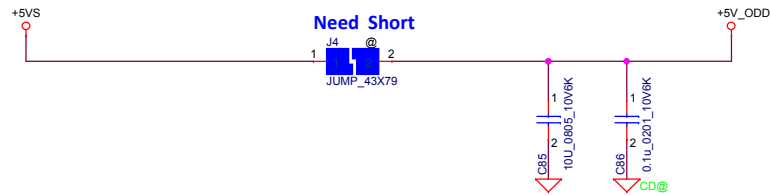
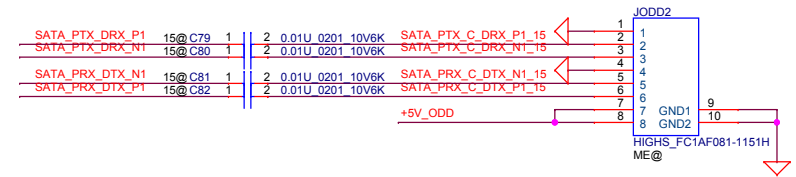
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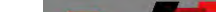
SATA HDD Conn.

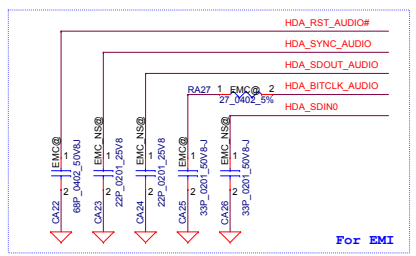
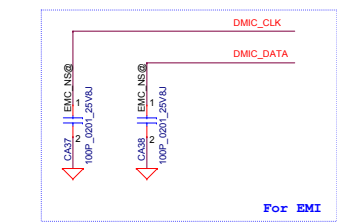
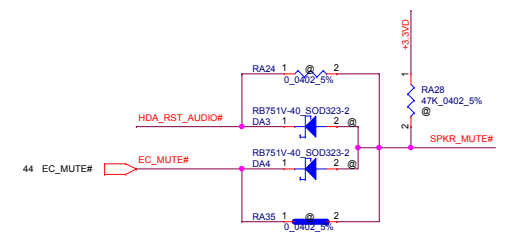
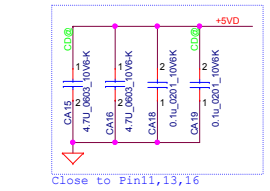
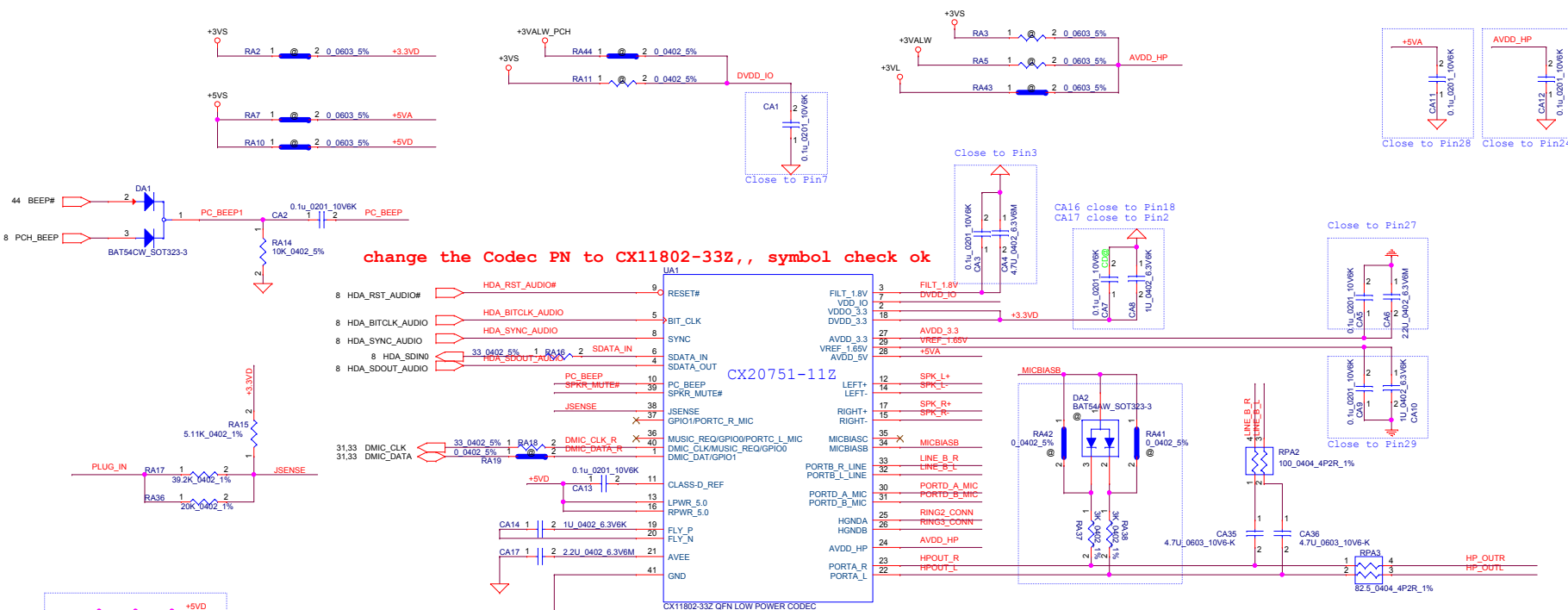
FOR 14"
SATA ODD Conn.



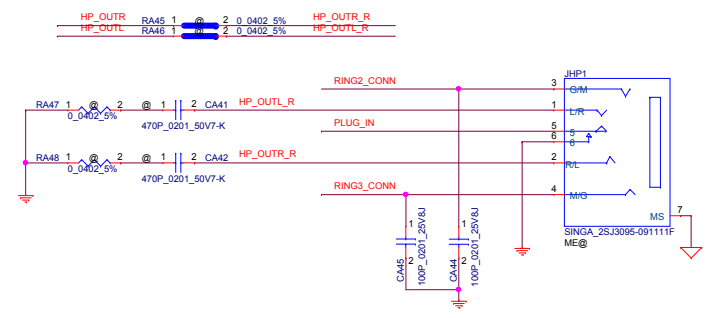
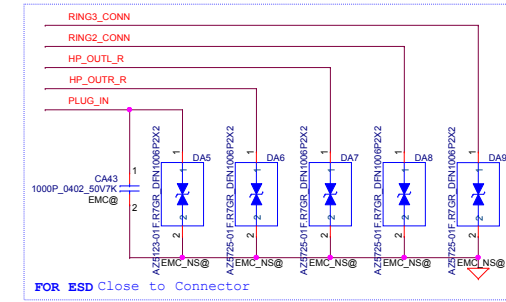
FOR 15"
SATA ODD FFC Conn



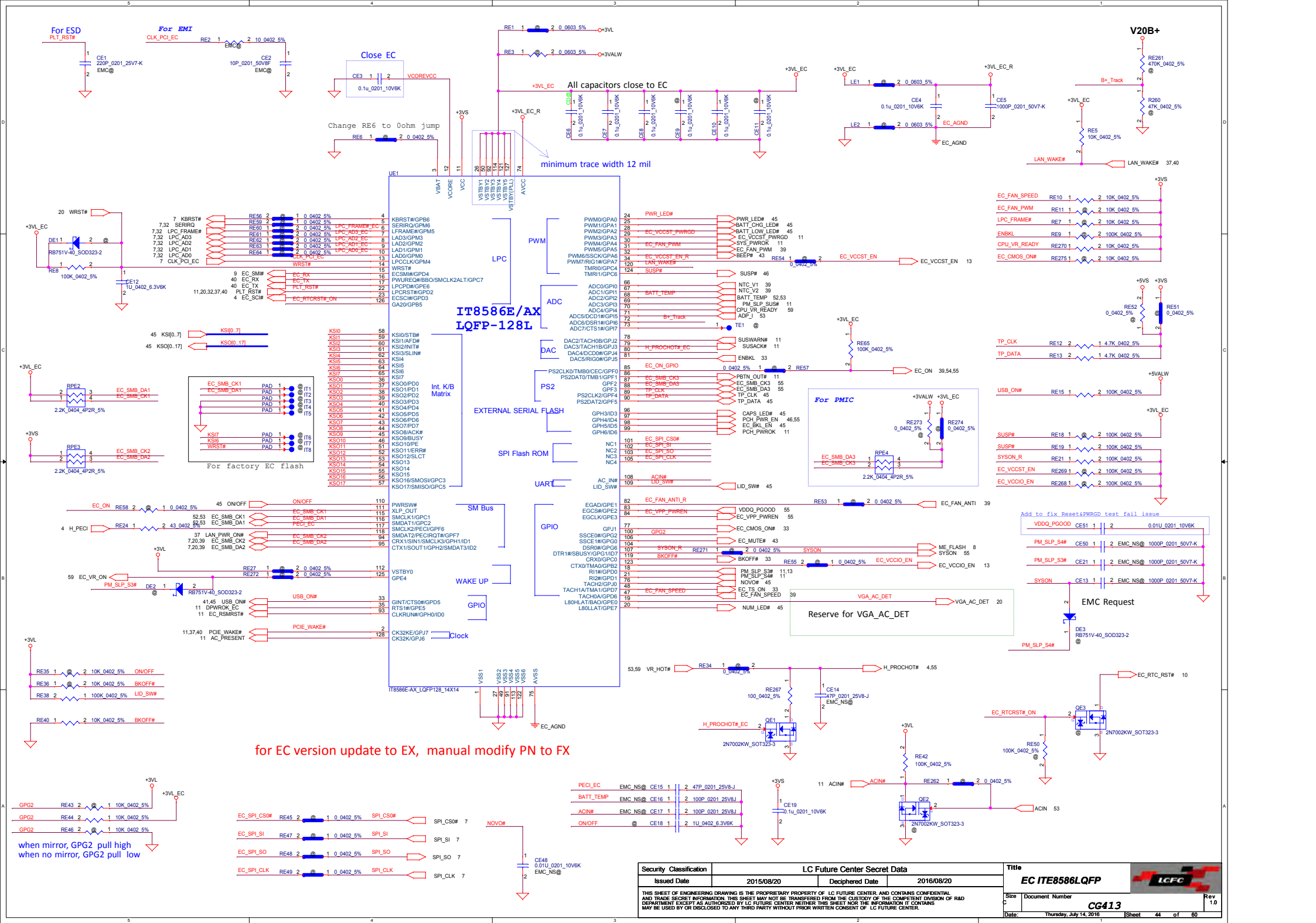
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Audio Jack



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Issued Date	2015/08/20	Deciphered Date	2016/08/20	Codec_CX11802 & Audio Jack	
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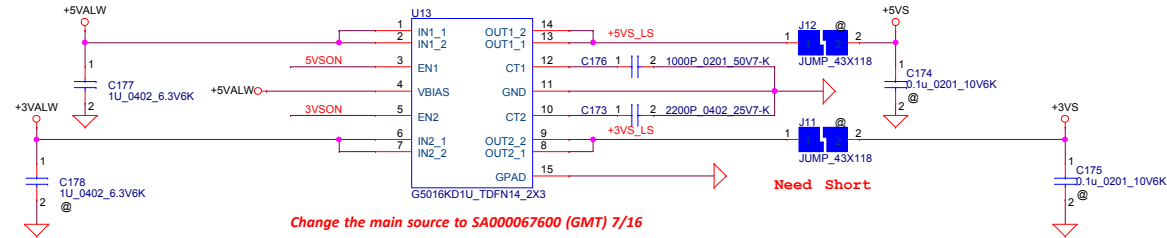
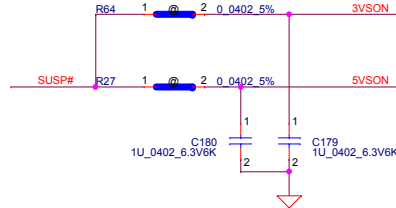


Load Switch **+5VALW To +5VS** **+3VALW To +3VS**

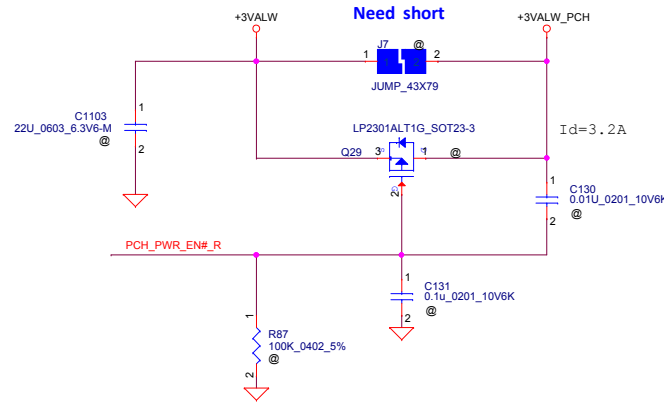
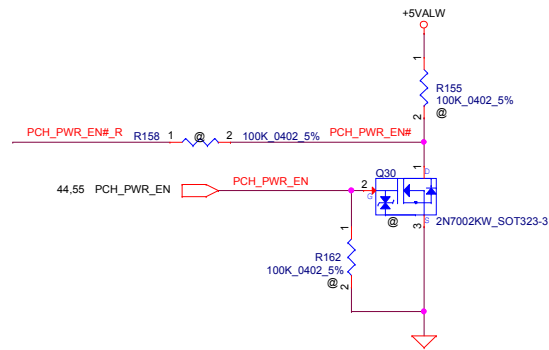
+3VS, C173 --> 2.74ms
+5VS, C176 --> 2.03ms

VIN 5V and 3.3V (VBIAS=5V), IMAX(per channel)=6A, Rds=16mohm

Need Short

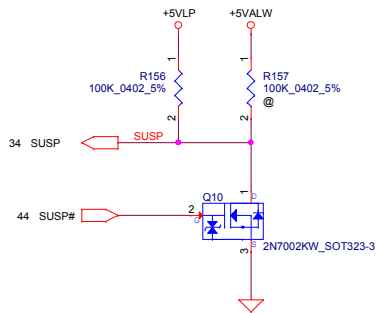


Change the main source to SA000067600 (GMT) 7/16

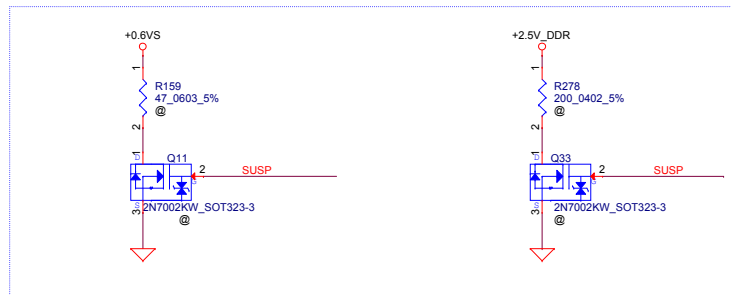


Need short

I_d=3.2A



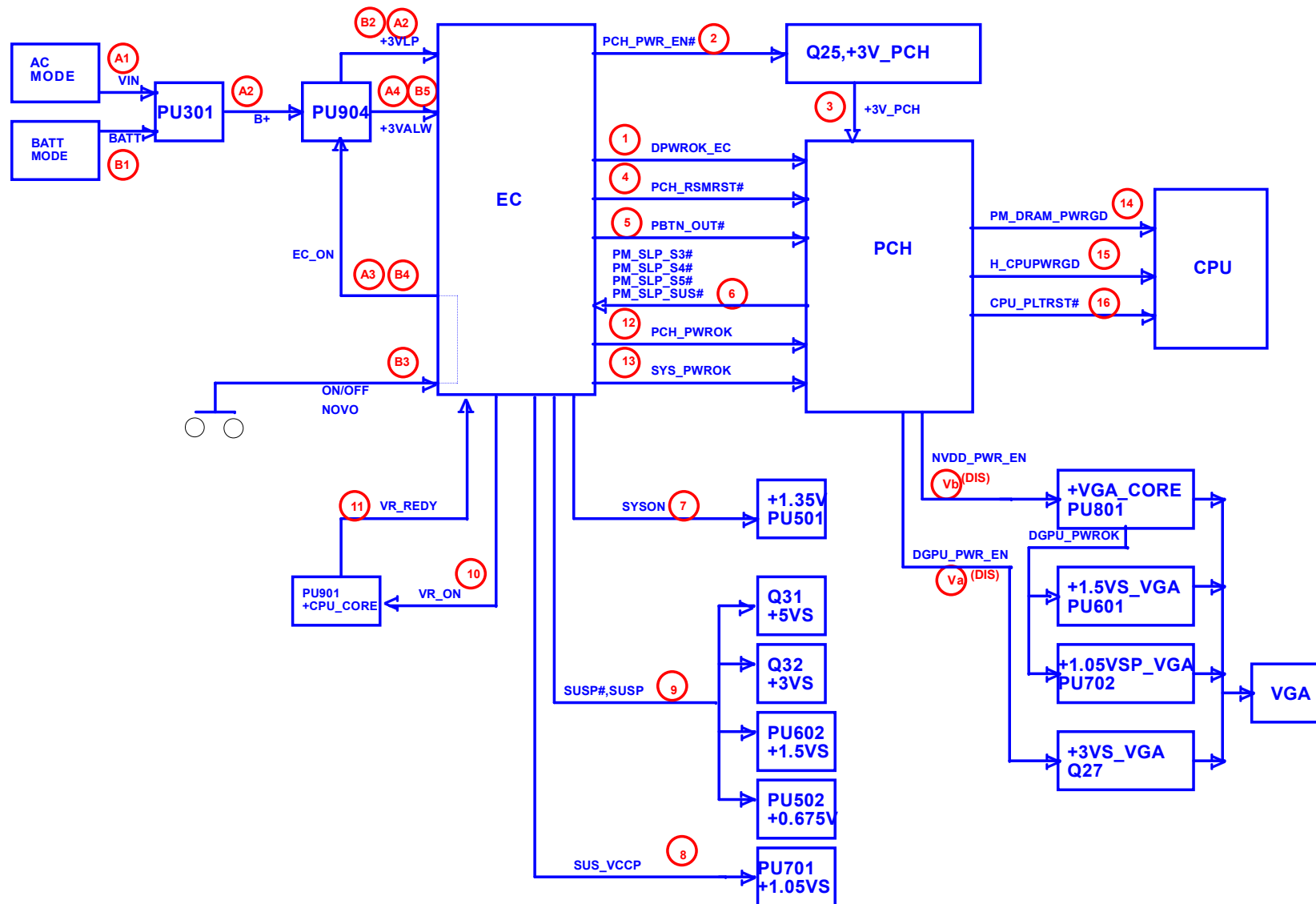
For DisCharge



08/29: Need double check enable signal and the resistance

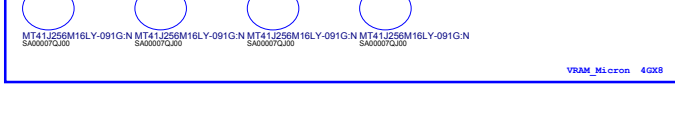
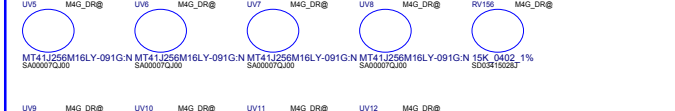
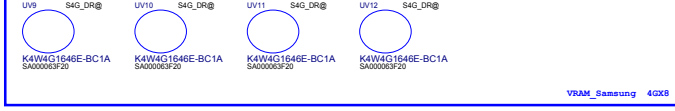
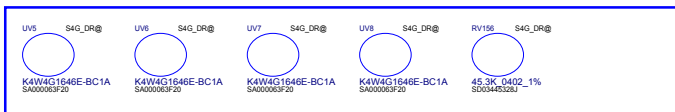
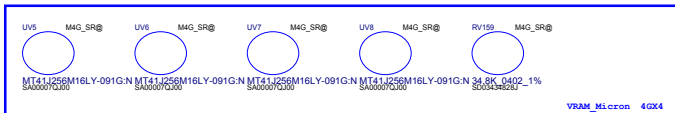
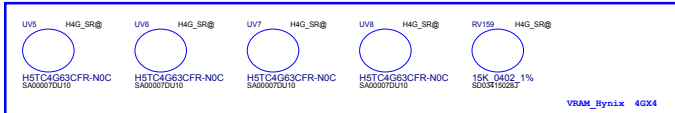
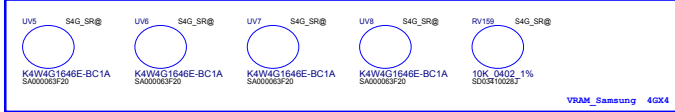
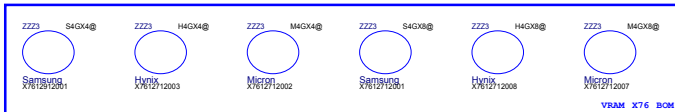
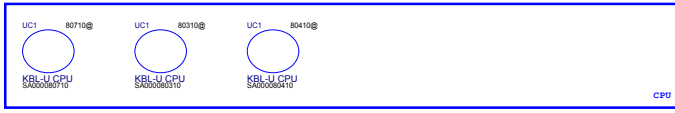
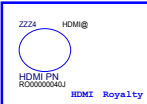
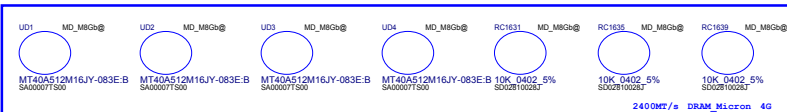
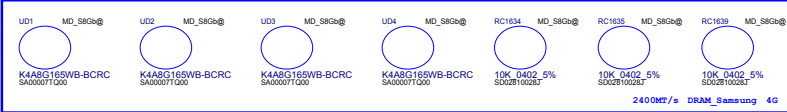
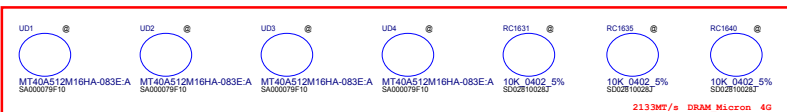
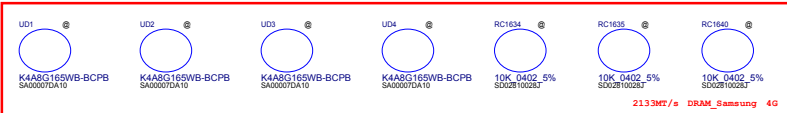
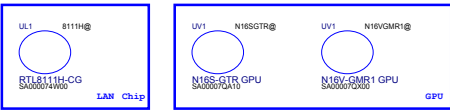
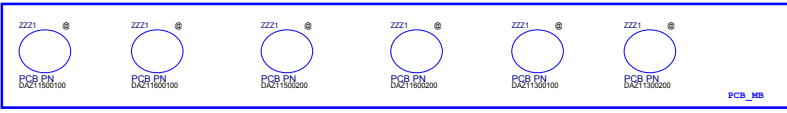
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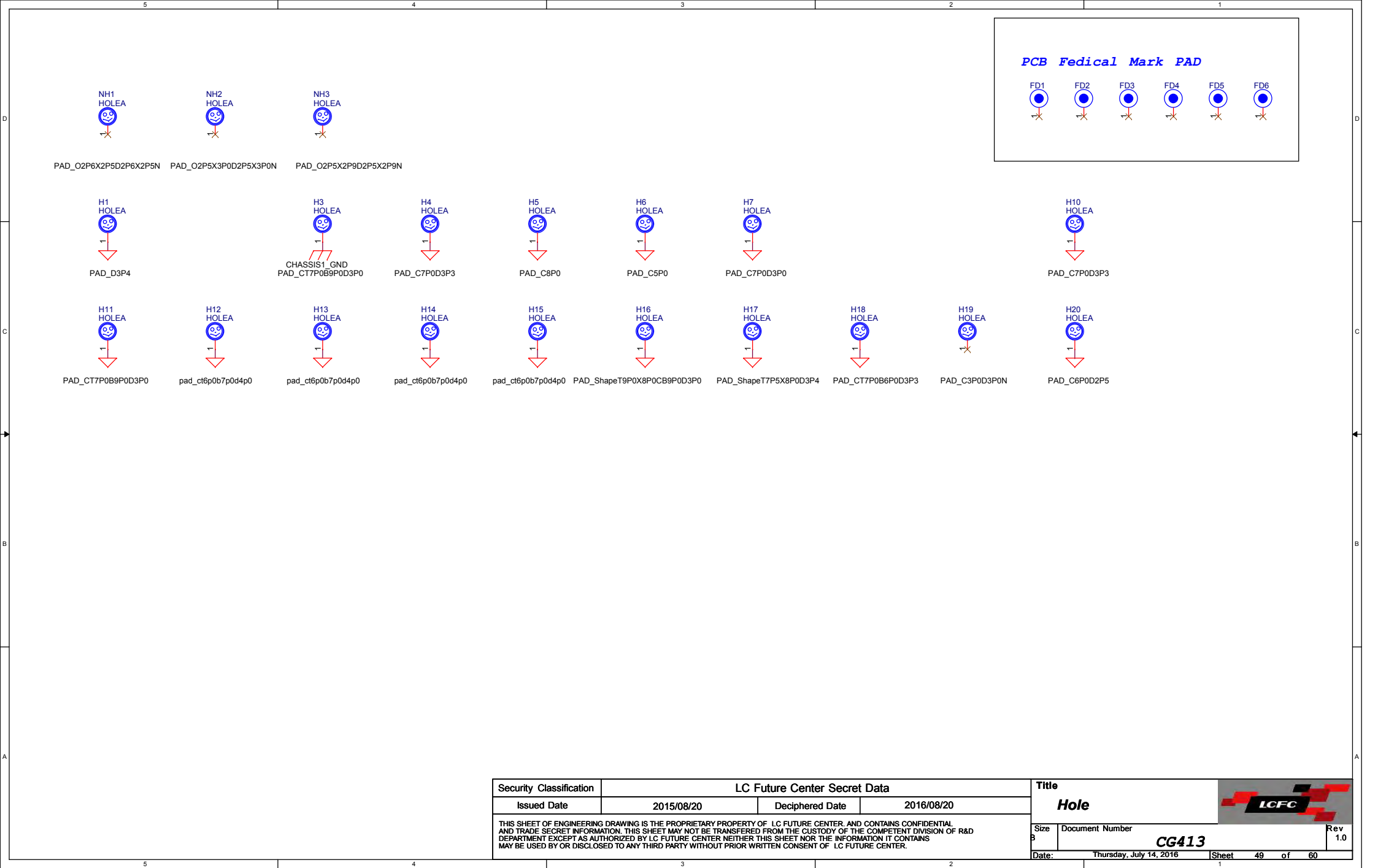
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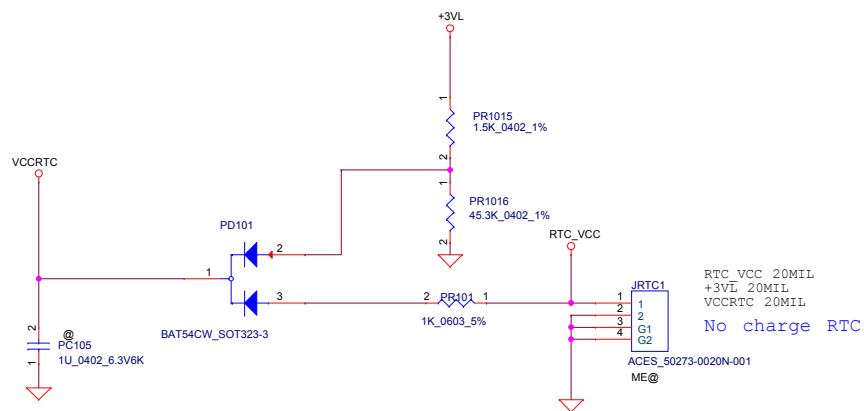
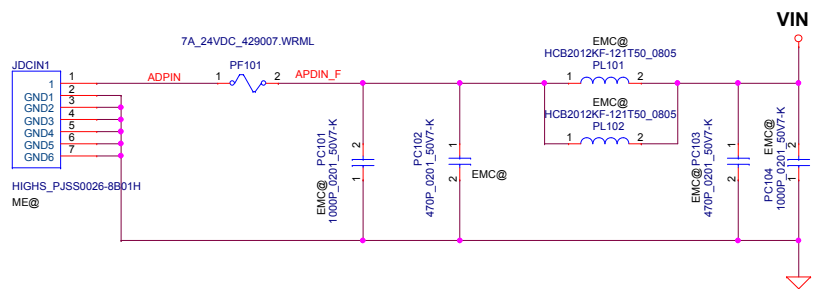


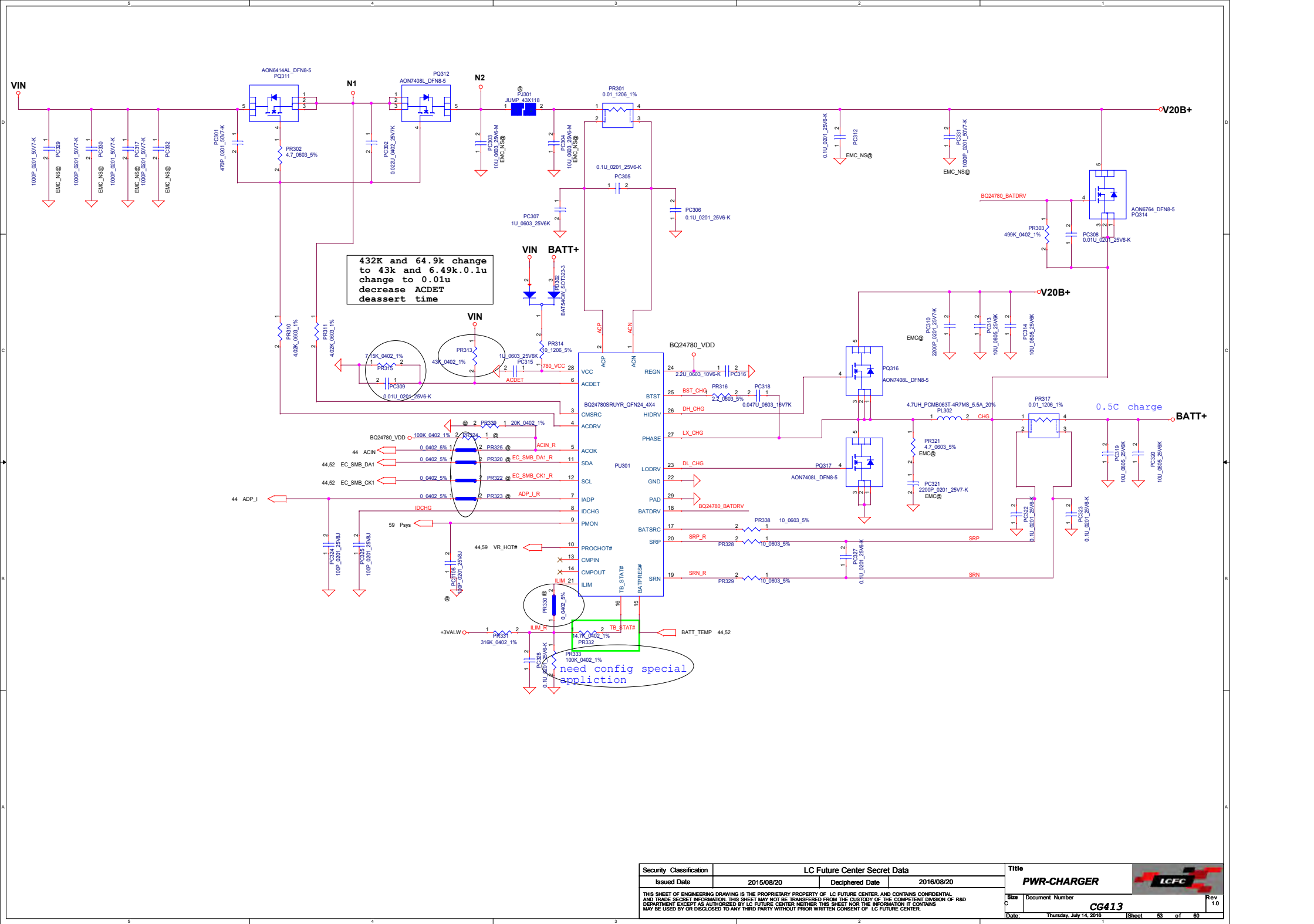
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Issued Date	2015/08/20	Deciphered Date	2016/08/20
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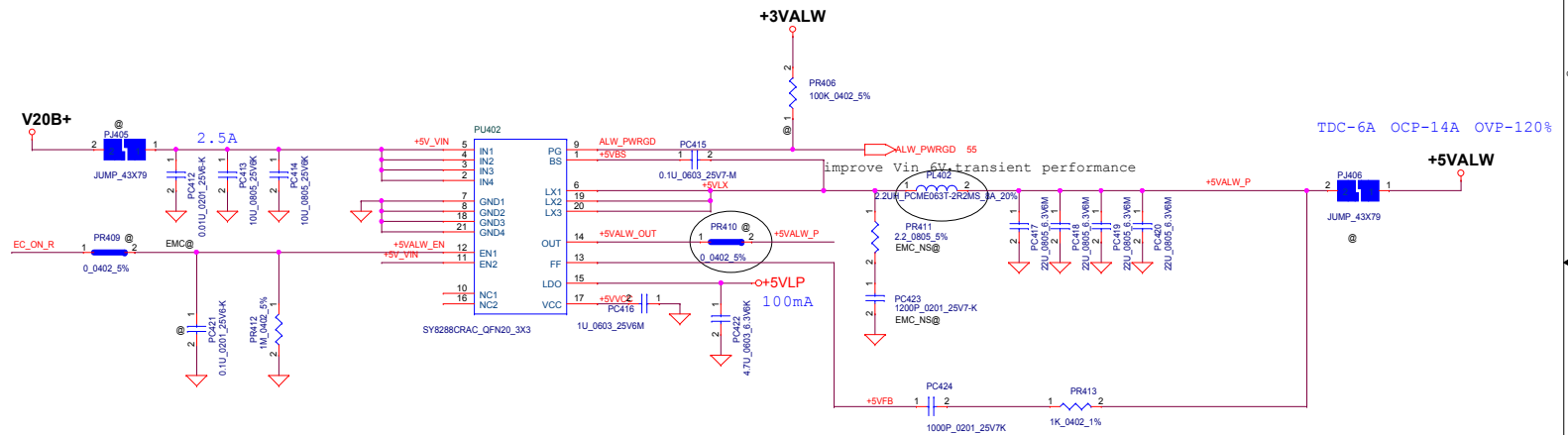
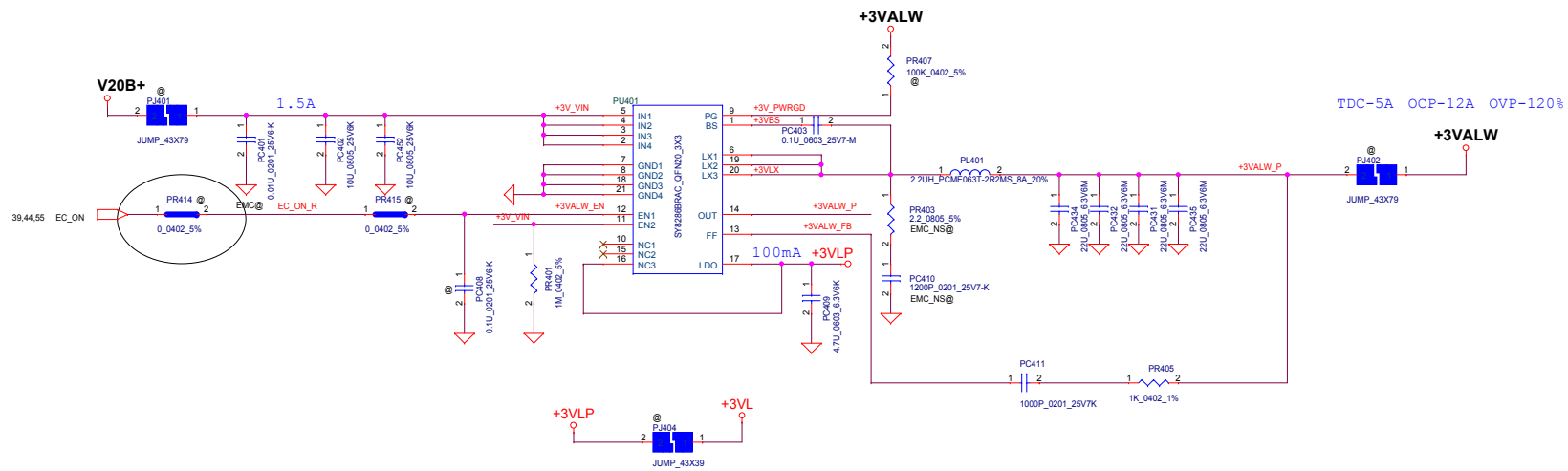
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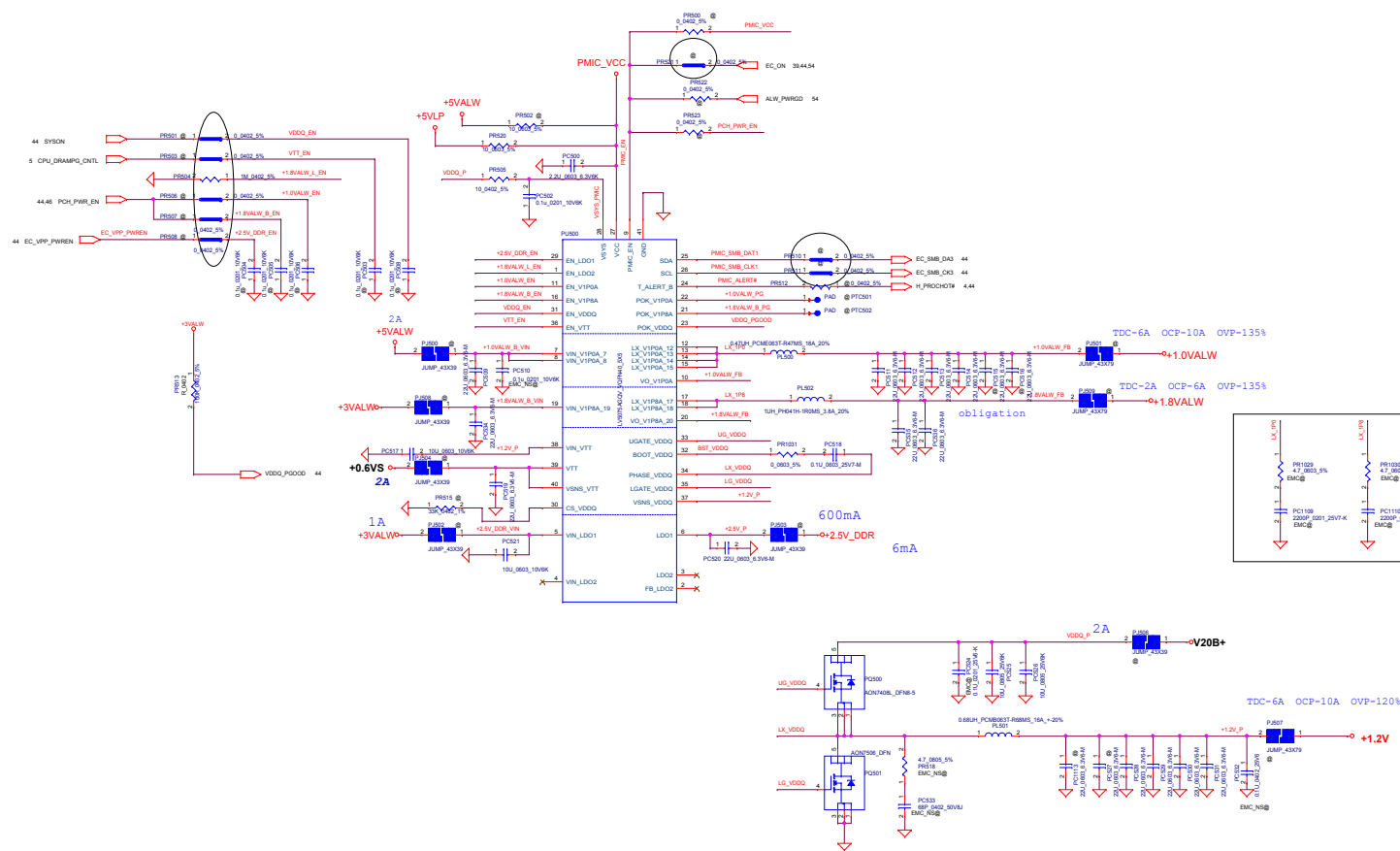




6800pf soft start 2ms
47nf soft start 7ms

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